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Project code :3PD00L010001
PCB No :13094
Revision :SB

Project Name :PIM81L/aMadrid
Size : 165x240mm

Madrid_SB Schematics Document

HASWELL INTEL LYNX POINT

Haswell LGA1150

aMadrid 195" UMA SKU : U,N,O
aMadrid 195" GPU SKU : U,N,O,G
aMadrid 23" UMA SKU : S,A,L,O
aMadrid 23" GPU SKU : S,A,L,G,O (unmount Q58)

S: Scalar
A: AMP
L : AspireLINK
G: GPU
O: OCP
N: non AMP
U: UMA(NOT S)
R: Unmount

OCP BOM manual control:
R439,R440,R441,R862 [63.R0031.16L]
Mount by BOM change list when w/o OCP

New P/N for manual control (1A):

manual control (SB):
23U : SCA1,DCIN2
23G : SCA1,VGA1

VGA1 : 071.0N15S.0B0U
SCA1 : 071.02586.000G
SKT2 : 022.70001.0121
DCIN2 : 22.10261.661

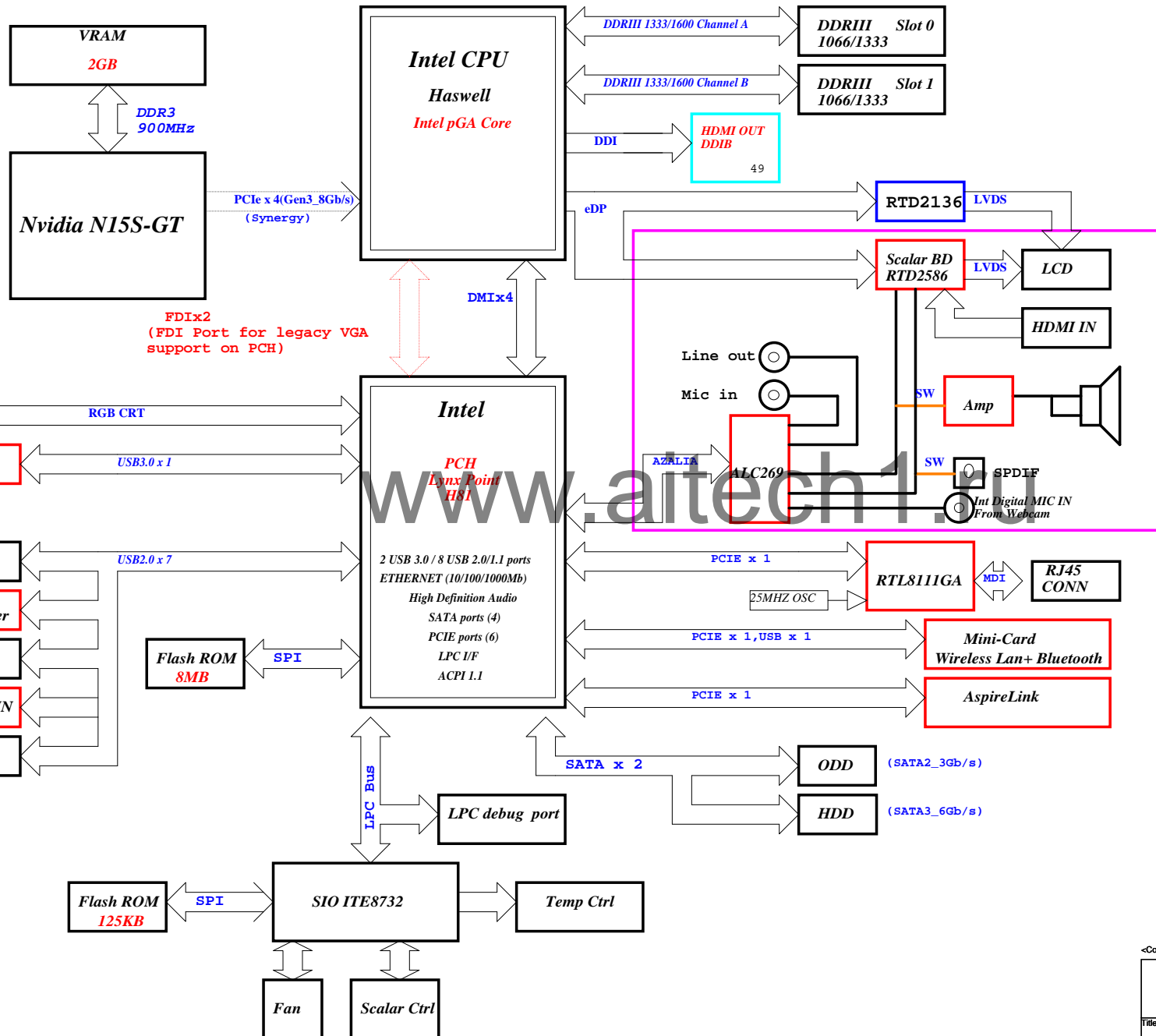
GPU SKU:
Hynix H5TC4G63AFR-11C
KN.0040G.002 -> R619=4.99K(64.49915.6DL)

Samsung K4W4G1646D-BC1A
KN.0040B.005 -> R619=15K(64.15025.6DL)

<Core Design>			
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Size Custom	Document Number Madrid		Rev SA
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Madrid Block Diagram (GPU)

Project code :3PD00L010001
PCB No :13094
Revision :SA
Project Name :Madrid



SYSTEM DC/DC RT8223MGQW 31	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_Charger 3D3V_A
CPU DC/DC ISL95832HRTZ 32~33	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC ISL95832HRTZ 34	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC ISL95870BHRZ 35	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC TPS51116RGER 36	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
LDO RT9025-25PSP 37	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
SYSTEM DC/DC TPS51461RGER 38	
INPUTS	OUTPUTS
5V_S5	0D85V_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

<Core Design>

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BLOCK DIAGRAM	
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PCH Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Leave floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: Connected to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

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DMI
11 DMI.IT_MR_DP[0..3] <<<>>>
11 DMI.IT_MR_DN[0..3] <<<>>>
11 DMI.IT_IR_DP[0..3] <<<>>>
11 DMI.IT_IR_DN[0..3] <<<>>>

FDI
11 FDI_CSYSNC <<<>>>
11 FDI_INT <<<>>>
11 FDI_TX_DN[0..1] <<<>>>
14 CK_DP_DP <<<>>>
14 CK_DP_DN <<<>>>

HDMIOUT
20131014 Madrid SA Charles
need HDMIOUT
44 DDSP_B_TX_DATA0 <<<>>>
44 DDSP_B_TX_DATA0# <<<>>>
44 DDSP_B_TX_DATA1 <<<>>>
44 DDSP_B_TX_DATA1# <<<>>>
44 DDSP_B_TX_DATA2 <<<>>>
44 DDSP_B_TX_DATA2# <<<>>>
44 DDSP_B_TX_DATA3 <<<>>>
44 DDSP_B_TX_DATA3# <<<>>>

EDP
To SCALAR & 2136 Colay
21 DPD_LANE0_S <<<>>>
21 DPD_LANE0P_S <<<>>>
21 DPD_LANE1_S <<<>>>
21 DPD_LANE1P_S <<<>>>

20131007 Madrid SA Charles
change Net to follow Pisa2
eDP Net Colay in Sheet 31,32,47

GPU PEG BUS
2013/04/03
Rossi delete PCIeX16 signal
20131010 Madrid SA Charles
checked p73

20131007 Madrid SA Charles
change Net to follow Pisa2
eDP Net Colay in Sheet 31,32,47

20131007 Madrid SA Charles
change Net to follow Pisa2
eDP Net Colay in Sheet 31,32,47

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Taipei Hsien 221, Taiwan, R.O.C.

File

CPU uLGA (DMI/FDI)

Rev

SA

Size

Document Number

Date

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of

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DDR DATA

9 M_A_DQ[0..63] <<< <<<
10 M_B_DQ[0..63] <<< <<<

9 M_A_DS[0..7] <<< <<<
9 M_A_DS[8..15] <<< <<<

10 M_B_DS[0..7] <<< <<<
10 M_B_DS[8..15] <<< <<<

DDR CMD/ADD

9 M_A_A[0..15] <<< <<<
10 M_B_A[0..15] <<< <<<

9 M_A_WE# <<< <<<
9 M_A_CAS# <<< <<<
9 M_A_RAS# <<< <<<
9 M_A_BS0 <<< <<<
9 M_A_BS1 <<< <<<
9 M_A_BS2 <<< <<<

10 M_B_WE# <<< <<<
10 M_B_CAS# <<< <<<
10 M_B_RAS# <<< <<<
10 M_B_BS0 <<< <<<
10 M_B_BS1 <<< <<<
10 M_B_BS2 <<< <<<

DDR CTRL

9 M_A_DIMM_CS#0 <<< <<<
9 M_A_DIMM_CS#1 <<< <<<

9 M_A_DIMM_CKE0 <<< <<<
9 M_A_DIMM_CKE1 <<< <<<

9 M_A_DIMM_ODT0 <<< <<<
9 M_A_DIMM_ODT1 <<< <<<

10 M_B_DIMM_CS#0 <<< <<<
10 M_B_DIMM_CS#1 <<< <<<

10 M_B_DIMM_CKE0 <<< <<<
10 M_B_DIMM_CKE1 <<< <<<

10 M_B_DIMM_ODT0 <<< <<<
10 M_B_DIMM_ODT1 <<< <<<

DDR CLOCK

9 M_A_DIMM_CLK_DDR0 <<< <<<
9 M_A_DIMM_CLK_DDR#0 <<< <<<
9 M_A_DIMM_CLK_DDR1 <<< <<<
9 M_A_DIMM_CLK_DDR#1 <<< <<<

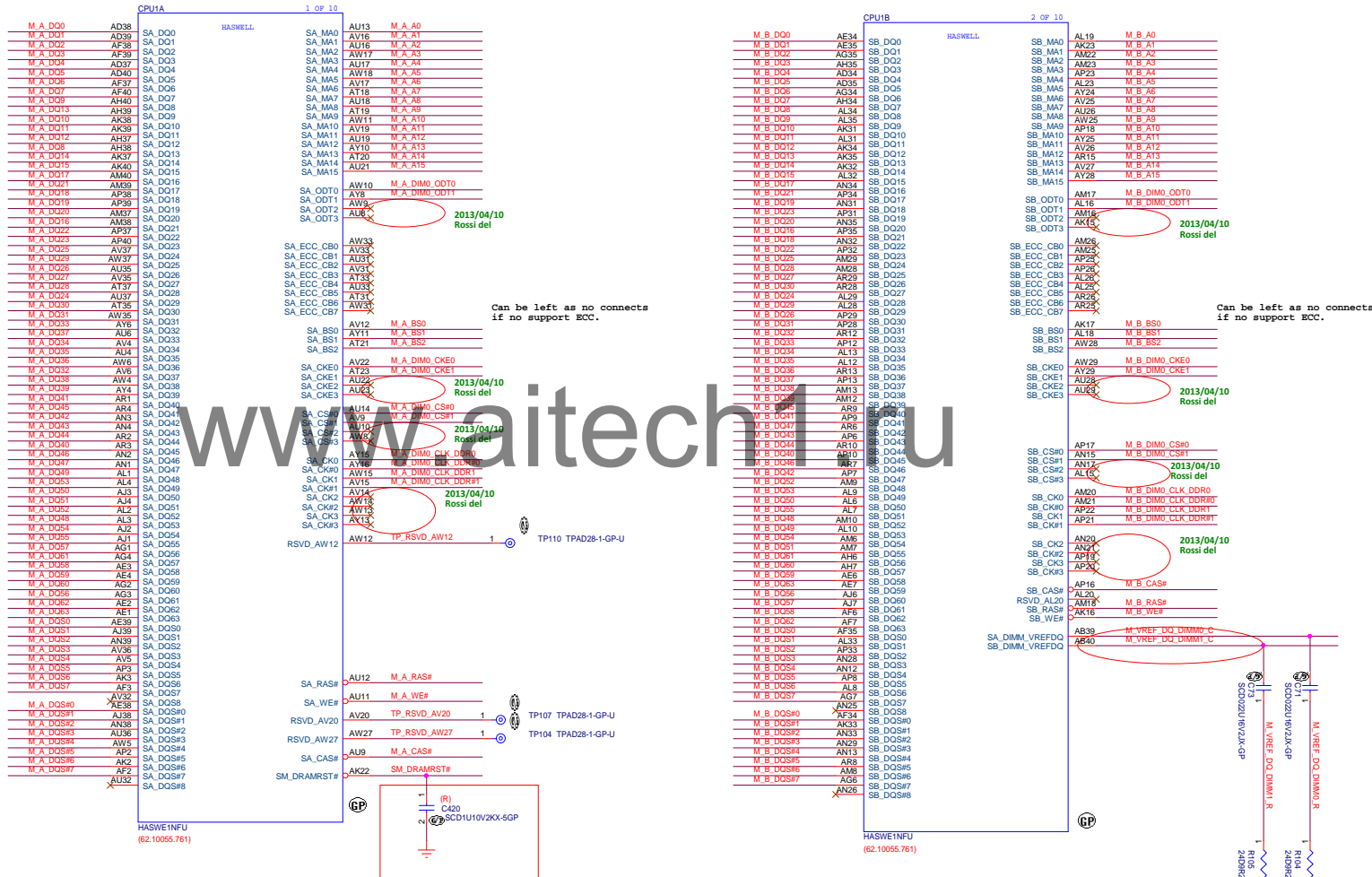
10 M_B_DIMM_CLK_DDR0 <<< <<<
10 M_B_DIMM_CLK_DDR#0 <<< <<<
10 M_B_DIMM_CLK_DDR1 <<< <<<
10 M_B_DIMM_CLK_DDR#1 <<< <<<

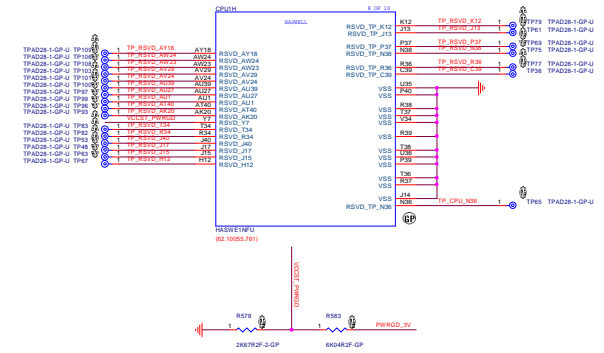
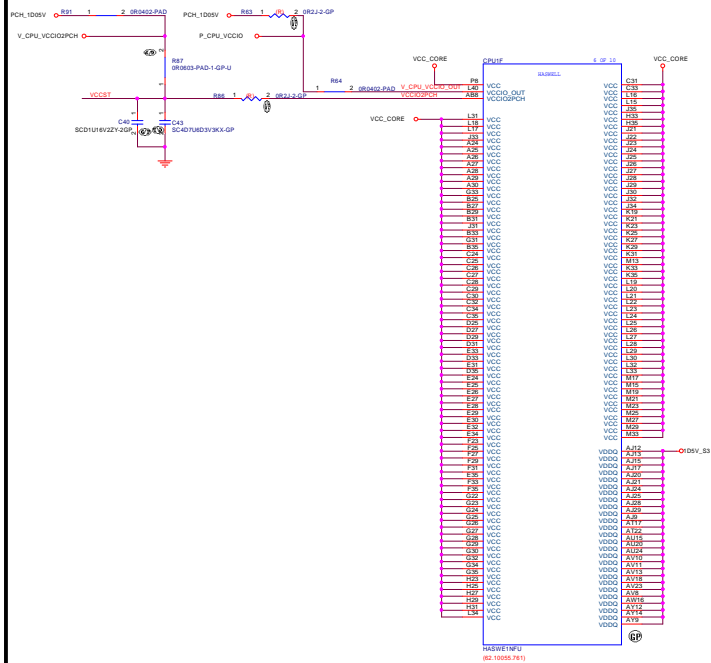
DDR OTHERS

33 SM_DRAMRST# <<< <<<
10 M_VREF_DQ_DIMM1_C <<< <<<
9 M_VREF_DQ_DIMM0_C <<< <<<

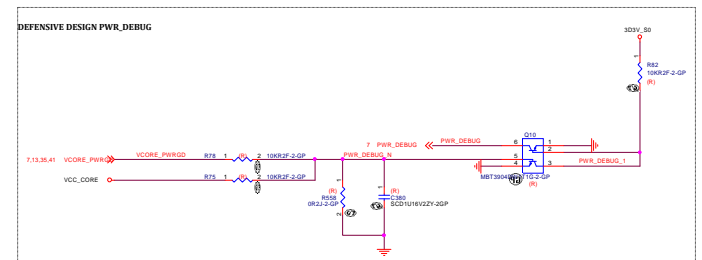
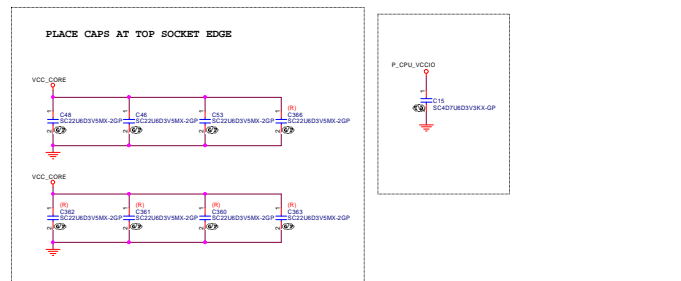
2013/04/10

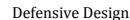
Rossi Change DIMM Net name reference swift



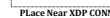


CPU Power	Capacitor	Quantity
Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)






continued...



1. Add DB (Dog Bone) only as needed on MS layer.
2. All segments are 50 Ω and vias are optional.
3. R1, R7 must be connected to the V_{SM} rail.
4. Connect components in Daisy-Chain topology in order to avoid stubs along the trace.
5. The layout topology guidelines remain the same whether the PCH or AND gate/buffer is driving the CPU.



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File	
CPU uLGA (VCORE/XDP)	
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Custom	Document Number
Madrid	
Date: 10/25/2010, January 21, 2014	Ebsent 7 of 8 SA

5 M_A_A[15:0] <<>>
5 M_A_DQS#[7:0] <<>>
5 M_A_DQS#[7:0] <<>>

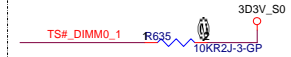
5 M_A_BS2 >>>
5 M_A_BS0
5 M_A_BS1
5 M_A_DQ[63:0]

2013/05/02
Rossi Change DIMM type follow London2
Symbol--> 62.10024.B81

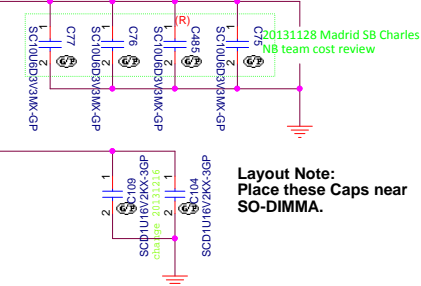
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

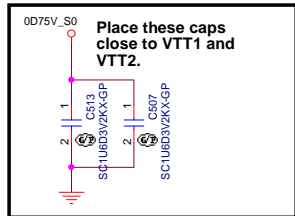
Thermal EVENT



SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA.



5 M_A_DIM0_ODT0 >>>
5 M_A_DIM0_ODT1 >>>

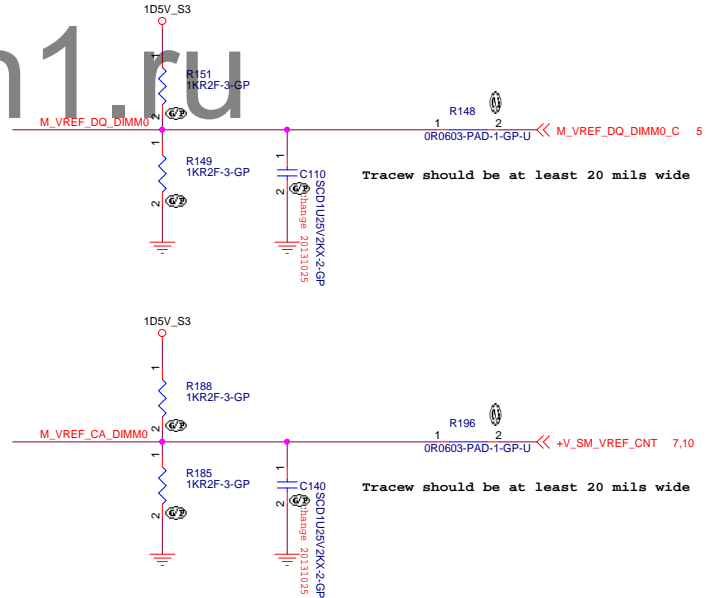
10,33 DDR3_DRAMRST# >>>

M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

0D75V_S0

H=8mm

DDR3-204P-101-GP-U
(62.10017.K01)



<Core Design>

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Title			DDR3-DIMM1	
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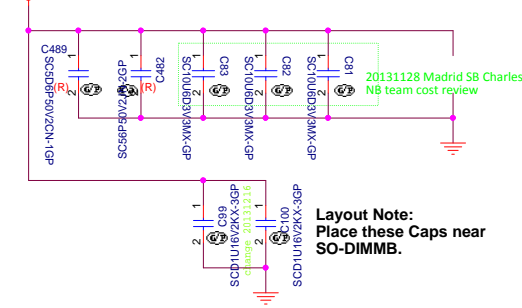
5 M_B_A[15:0] << >>
 5 M_B_DQS#[7:0] << >>
 5 M_B_DQS[7:0] << >>

2013/05/02
 Rossi Change DIMM type follow London2
 Symbol--> 62.10017.W31

Note:
 SO-DIMMB SPD Address is 0xA4
 SO-DIMMB TS Address is 0x34

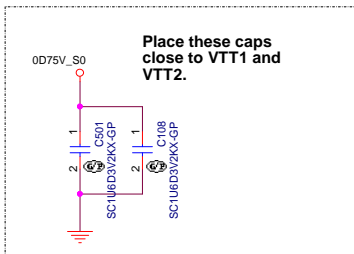
SO-DIMMB is placed farther from
 the Processor than SO-DIMMA

SODIMM B DECOUPLING

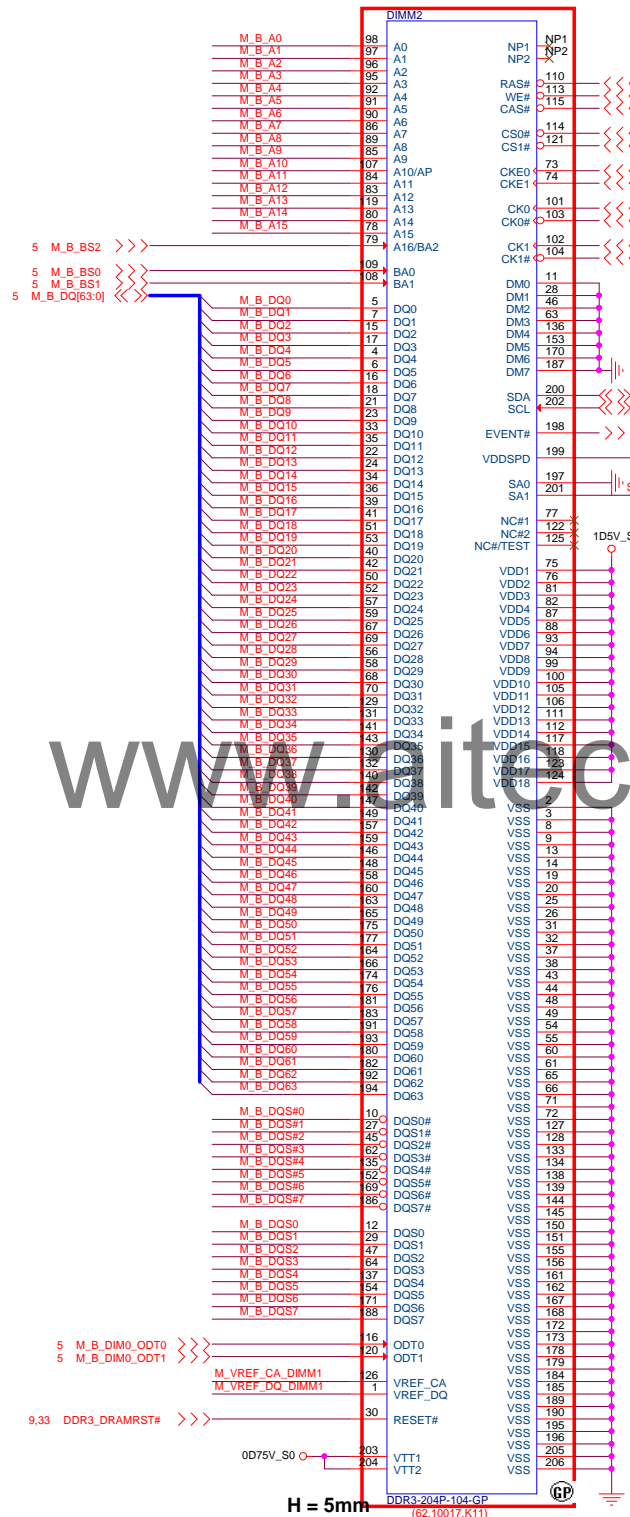


Layout Note:
 Place these Caps near
 SO-DIMMB.

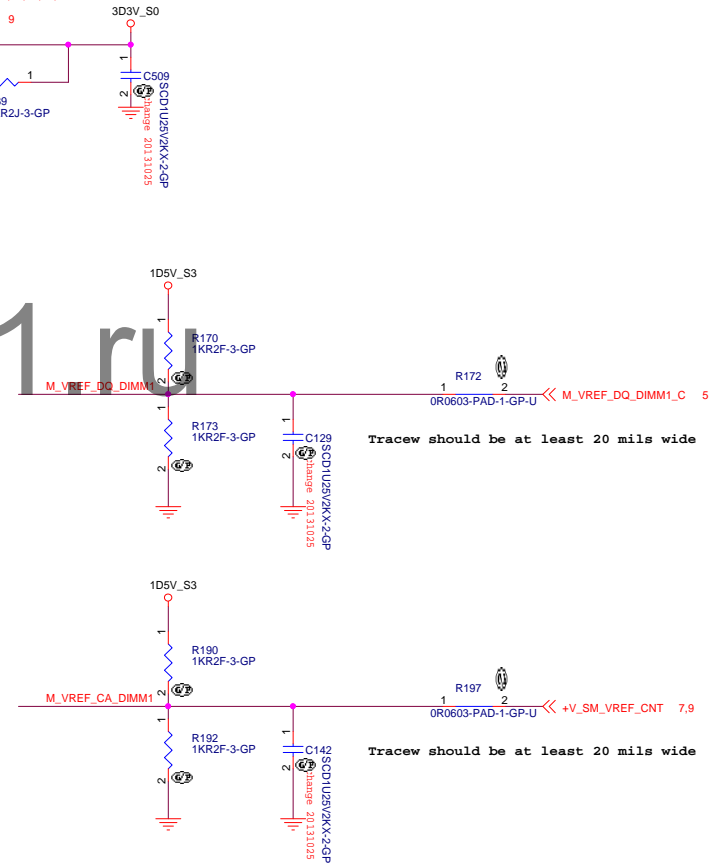
-2



Place these caps
 close to VTT1 and
 VTT2.



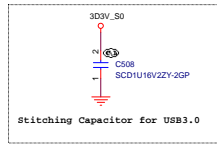
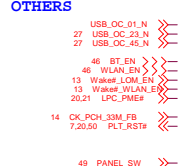
H = 5mm
 DDR3-204P-104-GP
 (62.10017.K11)



<Core Design>

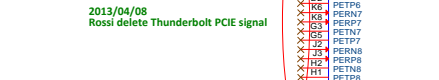
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Title DDR3-DIMM2		
Size Custom	Document Number Madrid	Rev SA
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OTHERS



20131010 Madrid SA Charles checked	DML MT_IR_DNU	L24	DML_RXNU
Connect to PCH 16,17	DML MT_IR_DP0	K24	DML_RXP0
	DML IT_MR_DNU	C20	DML_TXNU
	DML IT_MR_DP0	B20	DML_TXP0
	DML MT_IR_DNU1	G24	DML_RXNU1
	DML MT_IR_DNU2	H24	

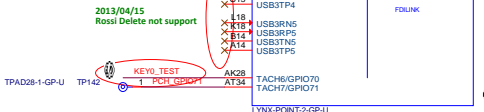
	Active	
DM1.MT.R.DND	L24	DM1.RXN0
DM1.MT.R.DND	L24	DM1.RXP0
DM1.MT.R.DND	G20	DM1.TXN0
DM1.MT.R.DND	G20	DM1.TXP0
DM1.MT.R.DND	G24	DM1.TXN1
DM1.MT.R.DND	G24	DM1.TXP1
DM1.MT.R.DND	G24	DM1.TXN2
DM1.MT.R.DND	G24	DM1.TXP2
DM1.MT.R.DND	G24	DM1.TXN3
DM1.MT.R.DND	G24	DM1.TXP3
DM1.MT.R.DND	G24	DM1.TXN4
DM1.MT.R.DND	G24	DM1.TXP4
DM1.MT.R.DND	G24	DM1.TXN5
DM1.MT.R.DND	G24	DM1.TXP5
DM1.MT.R.DND	G24	DM1.TXN6
DM1.MT.R.DND	G24	DM1.TXP6
DM1.MT.R.DND	G24	DM1.TXN7
DM1.MT.R.DND	G24	DM1.TXP7
DM1.MT.R.DND	G24	DM1.TXN8
DM1.MT.R.DND	G24	DM1.TXP8
DM1.MT.R.DND	G24	DM1.TXN9
DM1.MT.R.DND	G24	DM1.TXP9
DM1.MT.R.DND	G24	DM1.TXN10
DM1.MT.R.DND	G24	DM1.TXP10
DM1.MT.R.DND	G24	DM1.TXN11
DM1.MT.R.DND	G24	DM1.TXP11
DM1.MT.R.DND	G24	DM1.TXN12
DM1.MT.R.DND	G24	DM1.TXP12
DM1.MT.R.DND	G24	DM1.TXN13
DM1.MT.R.DND	G24	DM1.TXP13
DM1.MT.R.DND	G24	DM1.TXN14
DM1.MT.R.DND	G24	DM1.TXP14
DM1.MT.R.DND	G24	DM1.TXN15
DM1.MT.R.DND	G24	DM1.TXP15
DM1.MT.R.DND	G24	DM1.TXN16
DM1.MT.R.DND	G24	DM1.TXP16
DM1.MT.R.DND	G24	DM1.TXN17
DM1.MT.R.DND	G24	DM1.TXP17
DM1.MT.R.DND	G24	DM1.TXN18
DM1.MT.R.DND	G24	DM1.TXP18
DM1.MT.R.DND	G24	DM1.TXN19
DM1.MT.R.DND	G24	DM1.TXP19
DM1.MT.R.DND	G24	DM1.TXN20
DM1.MT.R.DND	G24	DM1.TXP20
DM1.MT.R.DND	G24	DM1.TXN21
DM1.MT.R.DND	G24	DM1.TXP21
DM1.MT.R.DND	G24	DM1.TXN22
DM1.MT.R.DND	G24	DM1.TXP22
DM1.MT.R.DND	G24	DM1.TXN23
DM1.MT.R.DND	G24	DM1.TXP23
DM1.MT.R.DND	G24	DM1.TXN24
DM1.MT.R.DND	G24	DM1.TXP24
DM1.MT.R.DND	G24	DM1.TXN25
DM1.MT.R.DND	G24	DM1.TXP25
DM1.MT.R.DND	G24	DM1.TXN26
DM1.MT.R.DND	G24	DM1.TXP26
DM1.MT.R.DND	G24	DM1.TXN27
DM1.MT.R.DND	G24	DM1.TXP27
DM1.MT.R.DND	G24	DM1.TXN28
DM1.MT.R.DND	G24	DM1.TXP28
DM1.MT.R.DND	G24	DM1.TXN29
DM1.MT.R.DND	G24	DM1.TXP29
DM1.MT.R.DND	G24	DM1.TXN30
DM1.MT.R.DND	G24	DM1.TXP30
DM1.MT.R.DND	G24	DM1.TXN31
DM1.MT.R.DND	G24	DM1.TXP31
DM1.MT.R.DND	G24	DM1.TXN32
DM1.MT.R.DND	G24	DM1.TXP32
DM1.MT.R.DND	G24	DM1.TXN33
DM1.MT.R.DND	G24	DM1.TXP33
DM1.MT.R.DND	G24	DM1.TXN34
DM1.MT.R.DND	G24	DM1.TXP34
DM1.MT.R.DND	G24	DM1.TXN35
DM1.MT.R.DND	G24	DM1.TXP35
DM1.MT.R.DND	G24	DM1.TXN36
DM1.MT.R.DND	G24	DM1.TXP36
DM1.MT.R.DND	G24	DM1.TXN37
DM1.MT.R.DND	G24	DM1.TXP37
DM1.MT.R.DND	G24	DM1.TXN38
DM1.MT.R.DND	G24	DM1.TXP38
DM1.MT.R.DND	G24	DM1.TXN39
DM1.MT.R.DND	G24	DM1.TXP39
DM1.MT.R.DND	G24	DM1.TXN40
DM1.MT.R.DND	G24	DM1.TXP40
DM1.MT.R.DND	G24	DM1.TXN41
DM1.MT.R.DND	G24	DM1.TXP41
DM1.MT.R.DND	G24	DM1.TXN42
DM1.MT.R.DND	G24	DM1.TXP42
DM1.MT.R.DND	G24	DM1.TXN43
DM1.MT.R.DND	G24	DM1.TXP43
DM1.MT.R.DND	G24	DM1.TXN44
DM1.MT.R.DND	G24	DM1.TXP44
DM1.MT.R.DND	G24	DM1.TXN45
DM1.MT.R.DND	G24	DM1.TXP45
DM1.MT.R.DND	G24	DM1.TXN46
DM1.MT.R.DND	G24	DM1.TXP46
DM1.MT.R.DND	G24	DM1.TXN47
DM1.MT.R.DND	G24	DM1.TXP47
DM1.MT.R.DND	G24	DM1.TXN48
DM1.MT.R.DND	G24	DM1.TXP48
DM1.MT.R.DND	G24	DM1



USB Table

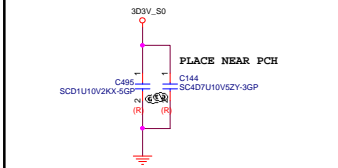
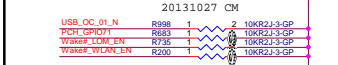
Pair	Device
0	USB3.0 Ext. port 1 (Side)
1	USB3.0 Ext. port 2 (Side)
2	Real USB2.0 ()
3	Real USB2.0 ()
4	Real USB2.0 ()
5	RF USB2.0 (Dual)
6	X
7	X
8	CR
9	Wireless LAN+BT
10	Touch
11	Webcam
12	X
13	X

HY (R465): TIE TRACES TOGETHER
IF NO LONGER THAN 1 INCH TO R



4. For pins that are available as GPIO-only: if the power-on default is Native, BIOS is still required to configure the pin as GPIO by writing to the pin's GPIO_USE_SEL register, even though the pin is only available as GPIO.

FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORT5
SOFT STRAP TO DETERMINE NATIVE FUNCTION



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH(FDI/PCIE/DMI/USB)			
Size	Document Number	Rev	
Custom	Madrid	S	
Date:	Tuesday, January 21, 2014	Sheet 11 of	68

Thermal shutdown

VGA

20131007 Madrid SA Charles
Madrid W/O VGA

SATA

HDD1
45 SATA_R0M
46 SATA_T0M
46 SATA_T0P

D0D1
45 SATA_R0M
46 SATA_T0M
46 SATA_T0P

OTHERS

7.54 H_PMI_SYNC_B
7.50 H_PMI_SYNC_A
6.1320 PWROD_3V
13 PCH_GPM_FU
30 H_ADGATE
20 INT_SERIRQ
7 PLTRST_CPU_LN
20 EC_SMB

ID

13 BOARD_ID_1
13 BOARD_ID_2

Straps

16 SATAGP
16 SATAGP
16 SATAGP

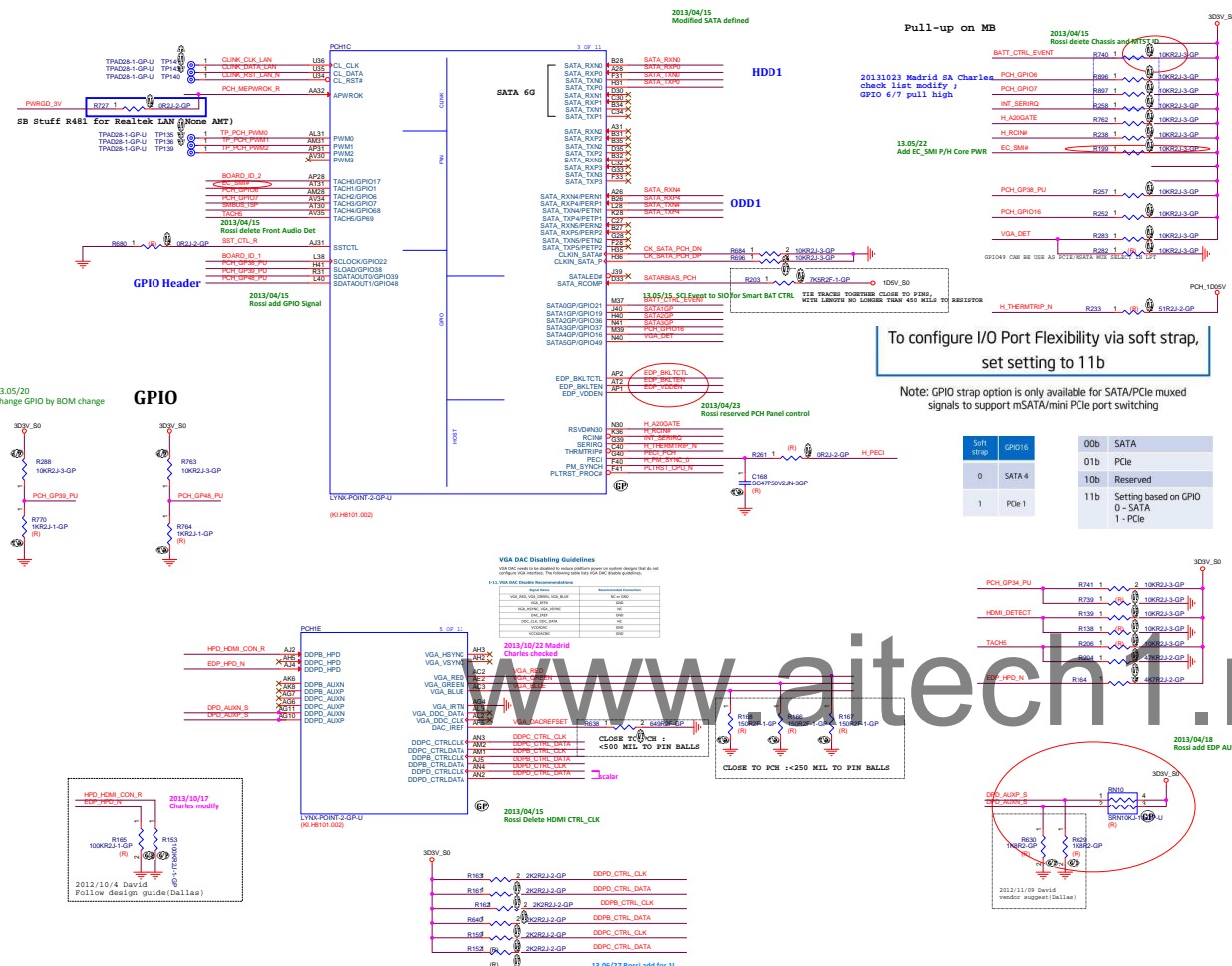
EDP

21 EDP_HPD_N
21 EDP_HPD_N
21 EDP_HPD_N
21.3223 EDP_BKCTL
23 EDP_BKCTL
23 EDP_VDDEN

4 HPD_HDMI_CON_R

20131007 Madrid SA Charles
P54 HDMIOUT

44 DOPR_CTRL_DATA
44 DOPR_CTRL_CLK



Feature Set	SKU Name					
	Intel® Q87 Express Chipset	Intel® Q85 Express Chipset	Intel® B85 Express Chipset	Intel® Z87 Express Chipset	Intel® H87 Express Chipset	Intel® H81 Express Chipset
Flexible I/O	Yes	No	No	Yes	Yes	No
PCI Express® 2.0 Ports	8 ⁴	8	8	8 ⁴	8 ⁴	6
Total number of USB ports	14	14	12 ⁵	14	14	10 ⁶
• USB 3.0 Capable Ports (SuperSpeed and all USB 2.0 speeds)	4(6) ⁷	4	4	4(6) ⁷	4(6) ⁷	2 ⁸
• USB 2.0 Only Ports	10(8) ⁹	10	8	10(8) ⁹	10(8) ⁹	8
Total number of SATA ports	4(6) ¹⁰	6	6	4(6) ¹⁰	4(6) ¹⁰	4 ¹¹
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	6	4 ¹²	4 ¹²	6	6	2 ¹³
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	0	2	2	0	0	2
VGA	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Wireless Display (WiDi)	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	No
Intel® Smart Response Technology ¹⁴	Yes	No	No	Yes	Yes	No
Intel® Anti-Theft Technology ¹⁵	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Active Management Technology 9.0	Yes	No	No	No	No	No
Intel® Small Business Advantage ¹⁶	Yes	Yes	Yes	No	Yes ¹⁷	No
Intel Rapid Start Technology ¹⁸	Yes	Yes	Yes	Yes	Yes	No
Intel® Identity Protection Technology (Intel® IPT) ¹⁹	Yes	Yes	Yes	Yes	Yes	Yes
Near Field Communication ²⁰	Yes	Yes	Yes	Yes	Yes	Yes
ACPI S1 State Support	Yes	Yes	Yes	Yes	Yes	Yes

- NOTES:**
- Contact your local Intel Field Sales Representative for currently available PCH SKUs.
 - Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
 - PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See Section 5.2.2 for more details.
 - The number of PCI Express ports available depends on the Flexible I/O configuration. See Section 2.7 and Table 1-3.
 - USB 2.0 ports 6 and 7 are disabled on 12 port SKUs.
 - USB 2.0 ports 6, 7, 12 and 13 are disabled on 10 port SKUs.
 - 6 USB 3.0 ports requires High Speed I/O ports 5 and 6 to be configured as USB 3.0. See Section 2.7 and Table 1-3.
 - Only USB 3.0 ports 1 and 2 are enabled.
 - When Flexible I/O ports are configured as USB 3.0, the total number of USB 2.0 only ports reduces in direct proportion.
 - 6 SATA ports requires High Speed I/O ports 13 and 14 to be configured as SATA. See Section 2.7 and Table 1-3.
 - SATA ports 2 and 3 are disabled on 4 port SKUs.
 - SATA 6 Gb/s support on ports 0, 1, 2 and 3. SATA ports 0, 1, 2 and 3 also support 3 Gb/s and 1.5 Gb/s.
 - SATA 6 Gb/s support on ports 0 and 1 only. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
 - Intel® Smart Response Technology requires Intel® Core™ processor.
 - Intel® Anti-Theft Technology requires an Intel® Core™ processor.
 - Intel® Small Business Advantage requires an Intel® Core™ processor.
 - Intel® Small Business Advantage with the Intel® H87 Express Chipset requires SMB firmware.
 - Intel® Rapid Start Technology requires an Intel® Core™ processor.
 - Intel® Identity Protection Technology requires an Intel® Core™ processor.
 - Near Field Communication is only supported in All-in-One system designs.

Wistron Corporation
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21F, No. 1, Hsin-Hua Rd., Hsinchu, Taiwan 30001, Taiwan, R.O.C.
PCH(SATA/FANDP/VGA)
Madrid
SA


```

50 CLK_PCI_LPC
11 CK_PCH_33M_FB
20 CLK_PCI_SIO

```

```

50 CLK_PCI_LPC
11 CK_PCH_33M_FB
20 CLK_PCI_SIO

```

```

7 CK_DPNS_R_DN
7 CK_DPNS_R_DP

7 CK_PE_100M_MCP_DN
7 CK_PE_100M_MCP_DP

4 CK_DP_DN
4 CK_DP_DP

```

```

7 CK_DPNS_R_DN
7 CK_DPNS_R_DP

7 CK_PE_100M_MCP_DN
7 CK_PE_100M_MCP_DP

4 CK_DP_DN
4 CK_DP_DP

```

```

25 CLK_PCIE_4_AspireLink#
25 CLK_PCIE_4_AspireLink

28 CK_PCIE_3_GLAN_DN
28 CK_PCIE_3_GLAN_DP

46 CLK_PCIE_WLAN
46 CLK_PCIE_WLAN#

```

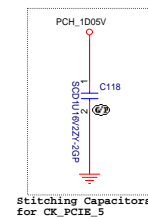
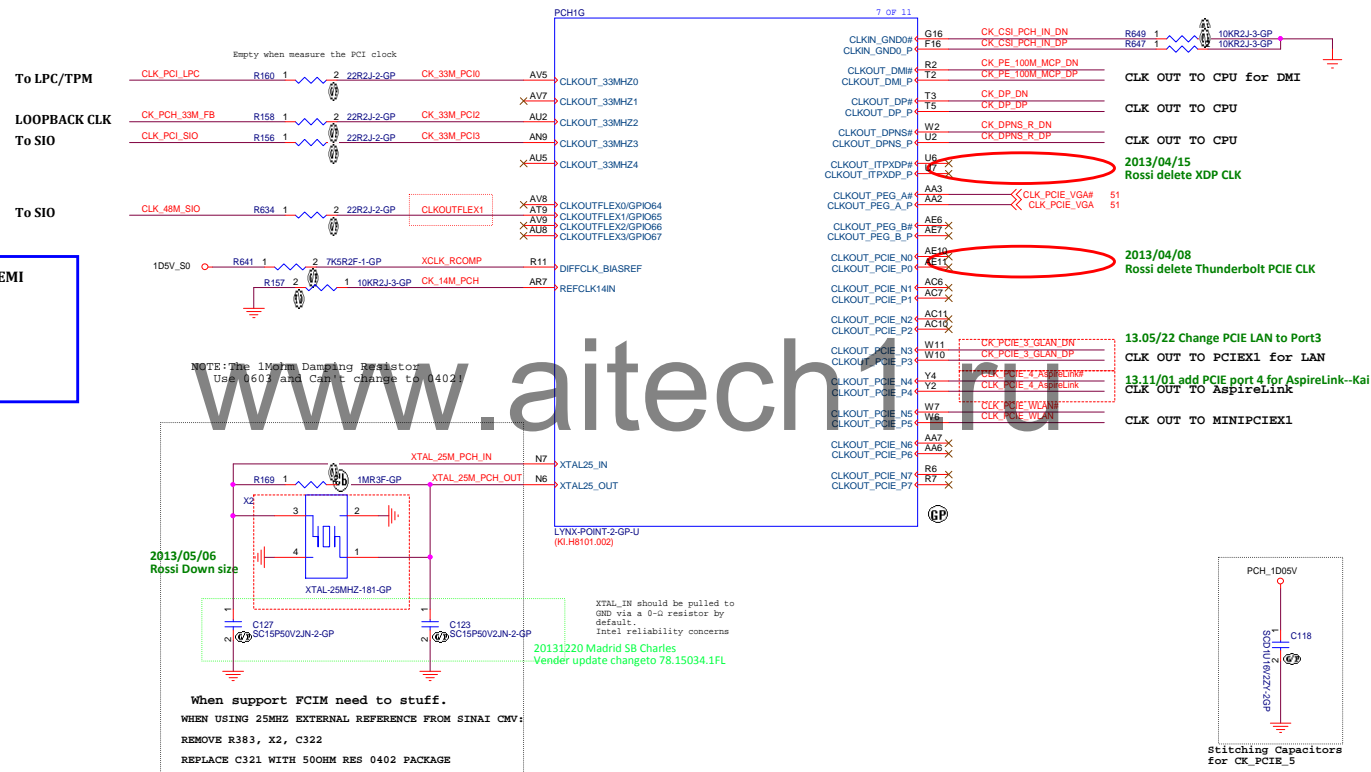
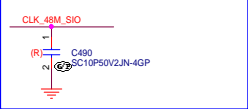
20 CLK_48M_SIO <<—

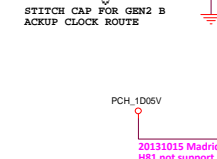
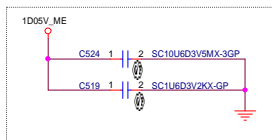
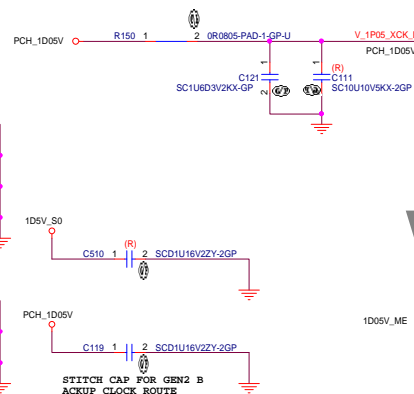
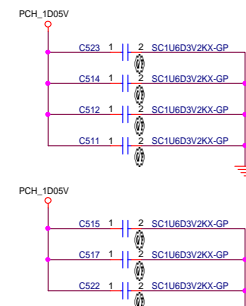
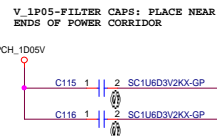
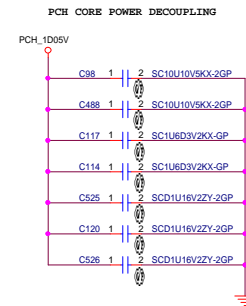
20 CLK_48M_SIO <<—

CLK_48M_SIO

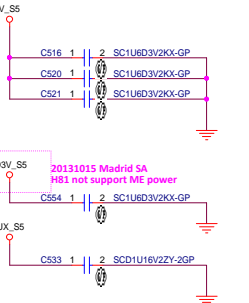
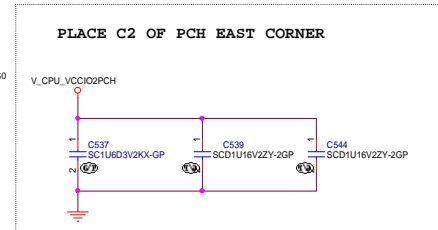
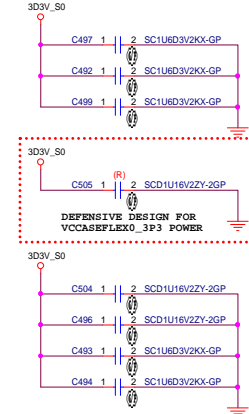
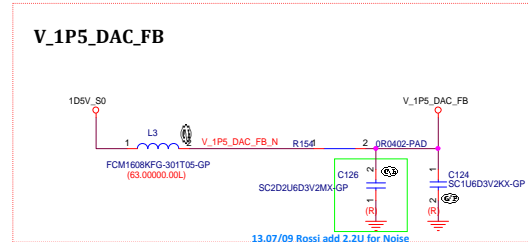
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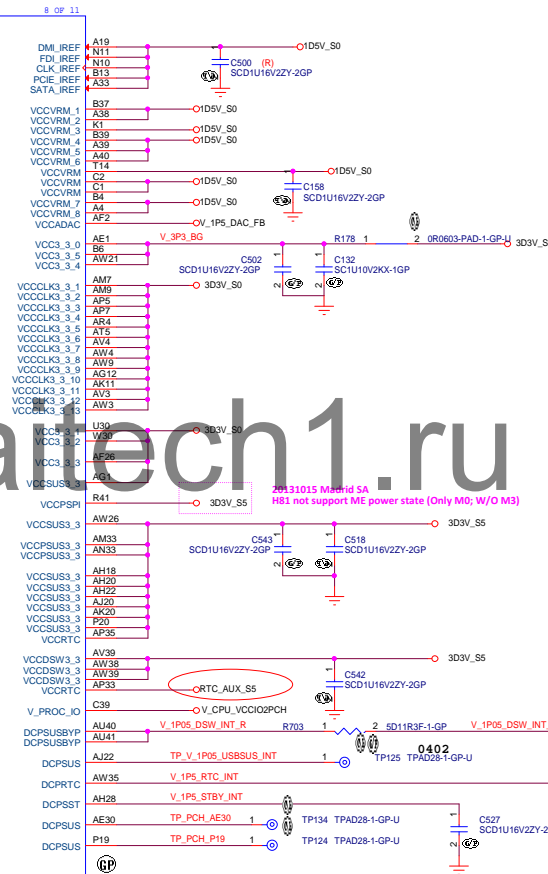




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H81 not support ME power



20131015 Madrid 5A
H81 not support ME power

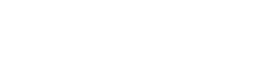
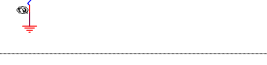
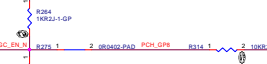
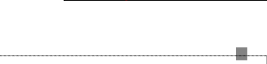
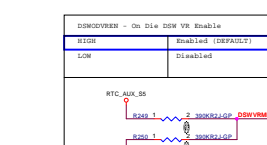
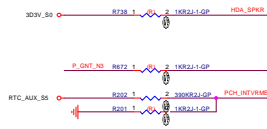


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INTVRMEN	Integrated VRM Enable	Always	<p>This signal does not have an internal resistor; an external resistor is required.</p> <p>0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only. Other systems should not pull the strap low.</p> <p>1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left floating.</p> <p>NOTES:</p> <ol style="list-style-type: none"> This signal is always sampled. This signal is in the RTC well.
----------	-----------------------	--------	--

STRAP

1	HSW_STRAP_13	
12	SATA2GP	
13	SATA2GP	
13	DSWVRMEN	
13	PCH_INTNVRMEN	
13.18	HDA_SPKR	
11	P_GNT_N0	
11	P_GNT_N1	
11	P_GNT_N2	



BOOT SELECT STRAPS

BOOT DEVICE	GP151 / GP1051	SATA2GP / GP1019
LPC	0	0
SPI	1	1

DESIGN NOTE:
WEAK INTERNAL PULLUPS ON GP151. DEFAULT SPI BOOT DEVICE.

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Strapping Pin define

Table 2-17. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
			This signal has a weak internal pull-up.
			This field determines the destination of accesses to the BIOS memory range. Also configurable using Boot BIOS Destination bit (Chapter Config Registers: Offset 3410h/Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.
			BIOS Bit 10 Destination
			0 = Disabled
			1 = Reserved
			2 = SPI (LPC)
			3 = Reserved
			4 = Reserved
			5 = Reserved
			6 = Reserved
			7 = Reserved
			8 = Reserved
			9 = Reserved
			10 = Reserved
			11 = Reserved
			12 = Reserved
			13 = Reserved
			14 = Reserved
			15 = Reserved
			16 = Reserved
			17 = Reserved
			18 = Reserved
			19 = Reserved
			20 = Reserved
			21 = Reserved
			22 = Reserved
			23 = Reserved
			24 = Reserved
			25 = Reserved
			26 = Reserved
			27 = Reserved
			28 = Reserved
			29 = Reserved
			30 = Reserved
			31 = Reserved

DESIGN NOTE:
The internal pull-up is disabled after PLTRST* deasserts.

DESIGN NOTE:
If option 0 (LPC) is selected, BIOS may still be shared on LPC, but the platform is required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.

DESIGN NOTE:
Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GME LAN.

DESIGN NOTE:
See Chapter 10, "I/OCS—General Control and Status Register" for additional information.

DESIGN NOTE:
The signal has a weak internal pull-up.

DESIGN NOTE:
This field determines the destination of accesses to the BIOS memory range. Also configurable using Boot BIOS Destination bit (Chapter Config Registers: Offset 3410h/Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.

DESIGN NOTE:
BIOS Bit 10 Destination

DESIGN NOTE:
0 = Disabled

DESIGN NOTE:
1 = Reserved

DESIGN NOTE:
2 = SPI (LPC)

DESIGN NOTE:
3 = Reserved

DESIGN NOTE:
4 = Reserved

DESIGN NOTE:
5 = Reserved

DESIGN NOTE:
6 = Reserved

DESIGN NOTE:
7 = Reserved

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DESIGN NOTE:
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DESIGN NOTE:
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DESIGN NOTE:
25 = Reserved

DESIGN NOTE:
26 = Reserved

DESIGN NOTE:
27 = Reserved

DESIGN NOTE:
28 = Reserved

DESIGN NOTE:
29 = Reserved

DESIGN NOTE:
30 = Reserved

DESIGN NOTE:
31 = Reserved

DESIGN NOTE:
The signal has a weak internal pull-up.

DESIGN NOTE:
This signal has a weak internal pull-up.

DESIGN NOTE:
The signal has a weak internal pull-up.

DESIGN NOTE:
The signal has a weak internal pull-up.

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DESIGN NOTE:
The signal has a weak internal pull-up.

DESIGN NOTE:
The signal has a weak internal pull-up.

Table 2-17. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
			This signal does not have an internal resistor; an external resistor is required.
			0 = Disable Integrated DeepSic Wall (DSW) On-Die Voltage Regulator.
			1 = Enable DSW 3.3V-to-1.05V Integrated DeepSic Wall (DSW) On-Die Voltage Regulator. This must always

19,21 SCALAR_OUT_R >> SCALAR_OUT_R
19,21 SCALAR_OUT_L >> SCALAR_OUT_L
CM 10/16
27 CODEC_LINE_IN_SENSE >> CODEC_LINE_IN_SENSE

HD_LINK
13 HDA_SDN0 >>
13 HDA_CODEC_SDOOUT >>
13,18,19 HDA_CODEC_RST# >>
13 HDA_CODEC_SYNC >>
13 HDA_CODEC_BITCLK >>

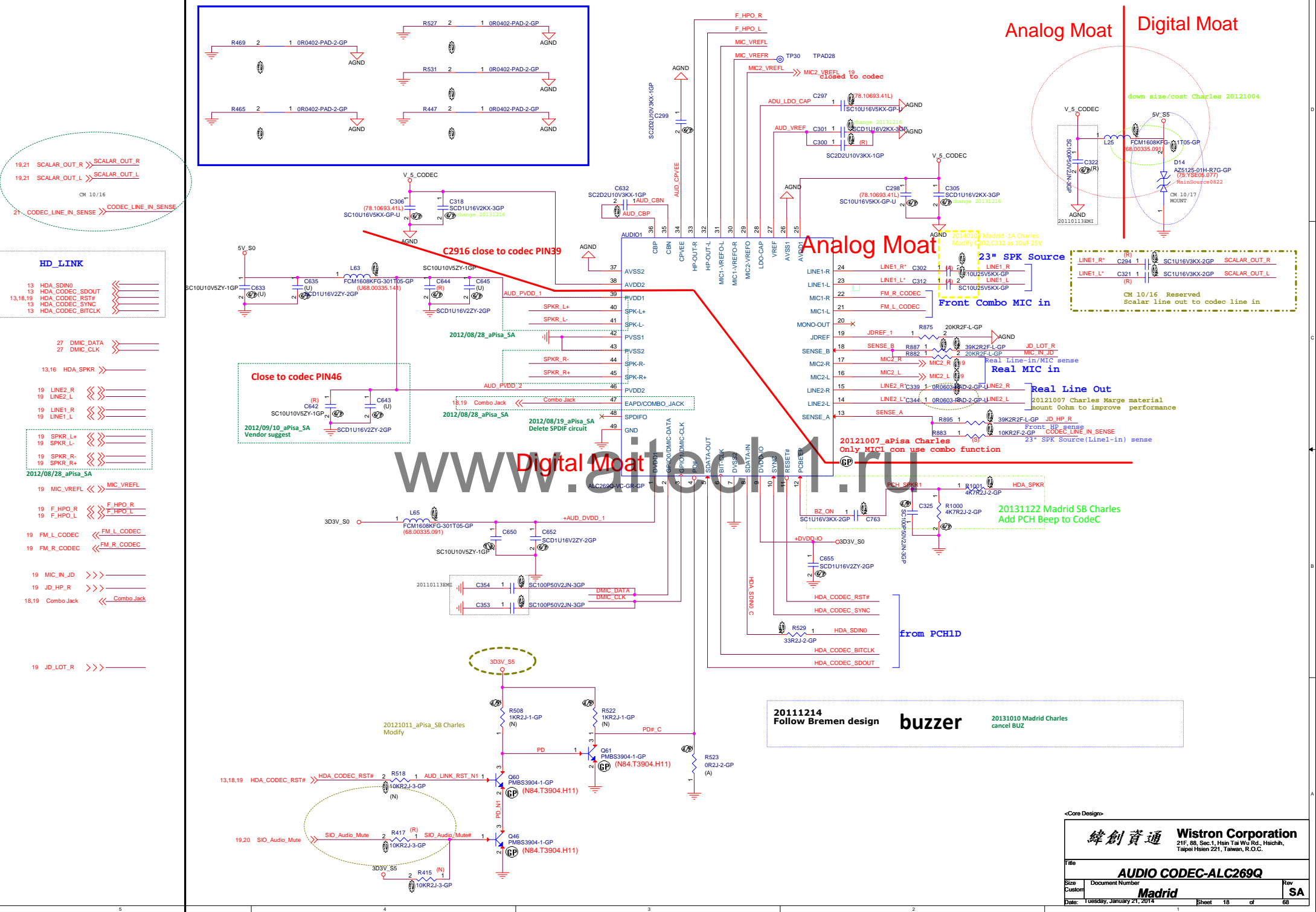
27 DMIC_DATA >>
27 DMIC_CLK >>
13,16 HDA_SPKR >>
19 LINE2_R >>
19 LINE2_L >>
19 LINE1_R >>
19 LINE1_L >>

19 SPKR_L+ >>
19 SPKR_L- >>
19 SPKR_R+ >>
19 SPKR_R- >>
2012/08/28 aPisa_SA

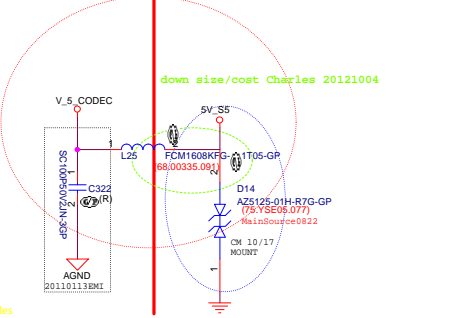
19 MIC_VREFL >> MIC_VREFL
19 F_HPO_R >> F_HPO_R
19 F_HPO_L >> F_HPO_L
19 FM_L_CODEC >> FM_L_CODEC
19 FM_R_CODEC >> FM_R_CODEC

19 MIC_IN_ID >>
19 JD_HP_R >>
18,19 Combo Jack >> Combo Jack

19 JD_LOT_R >>>



Analog Moat Digital Moat



Analog Moat

23" SPK Source
Front Combo MIC in

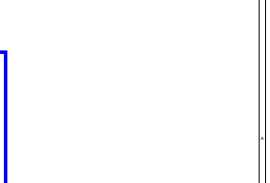
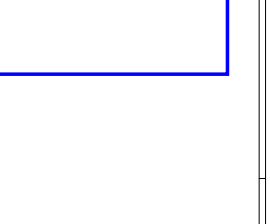
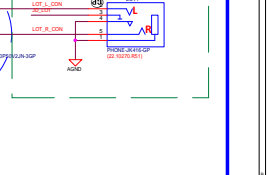
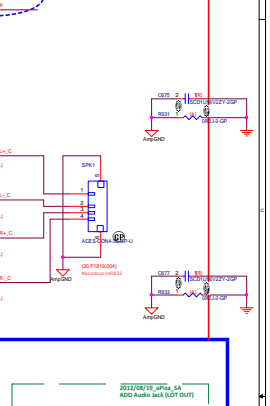
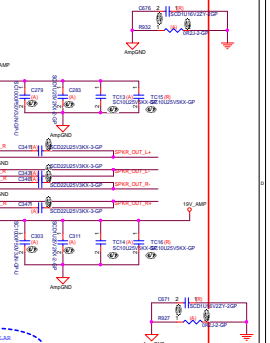
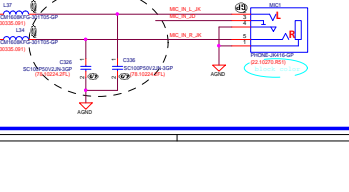
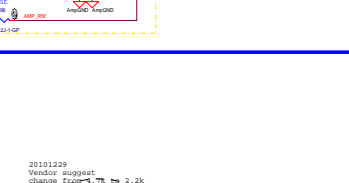
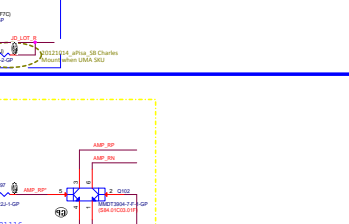
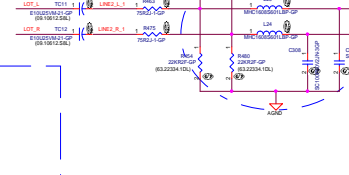
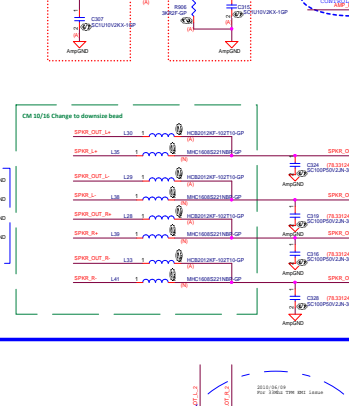
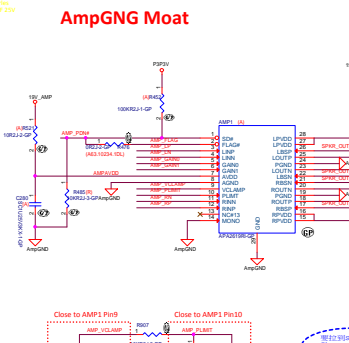
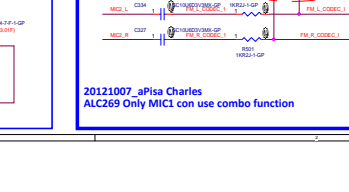
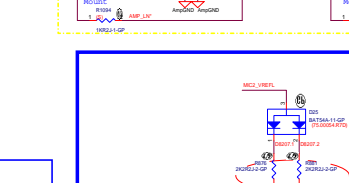
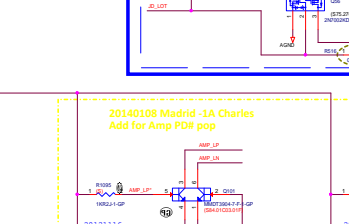
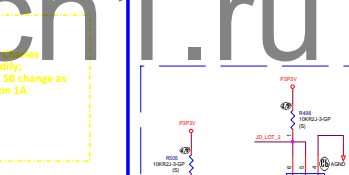
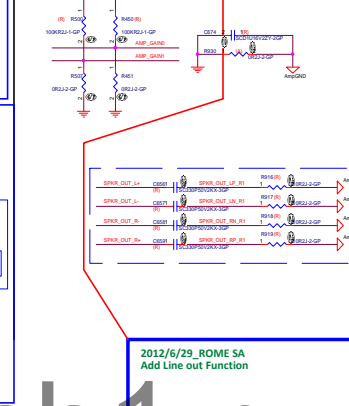
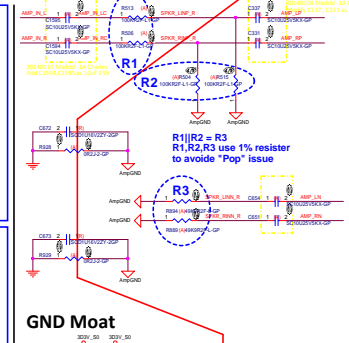
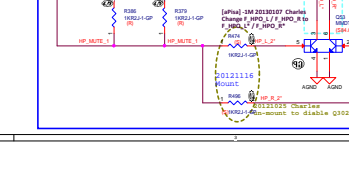
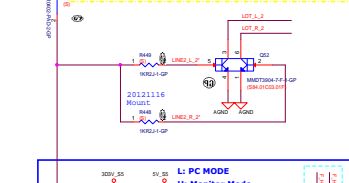
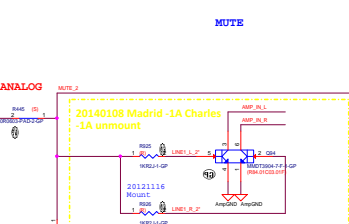
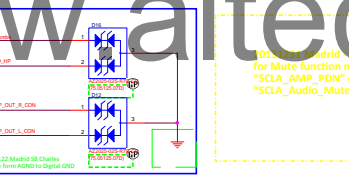
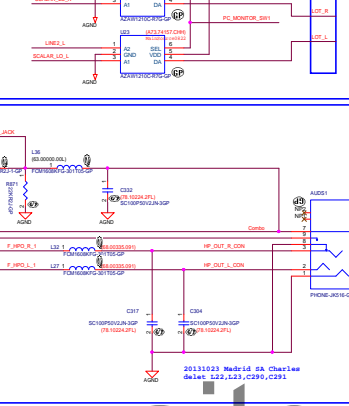
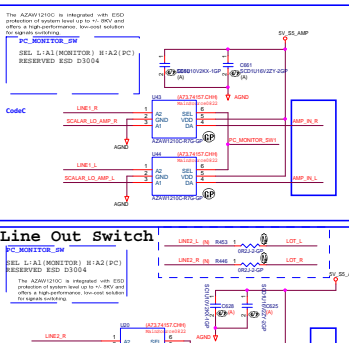
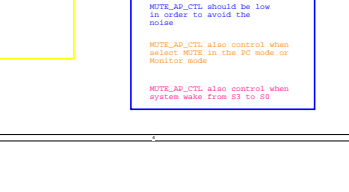
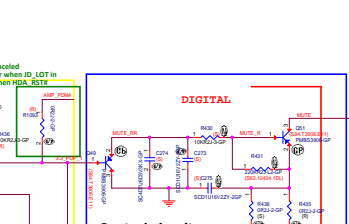
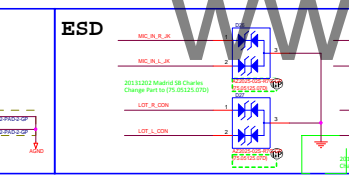
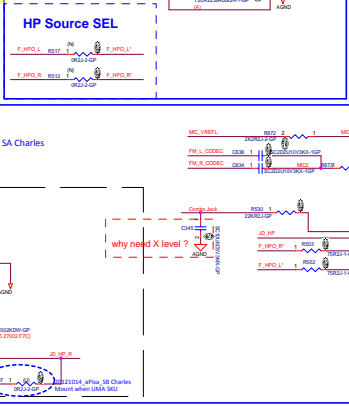
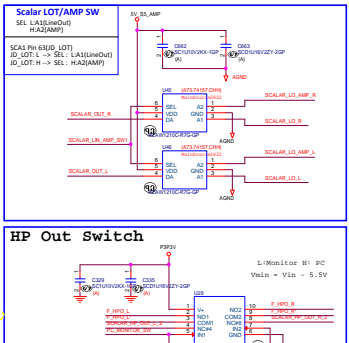
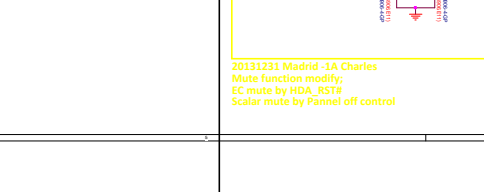
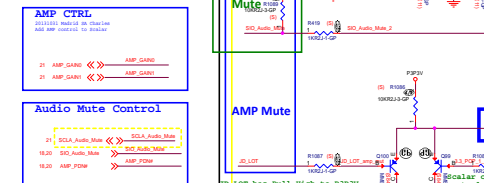
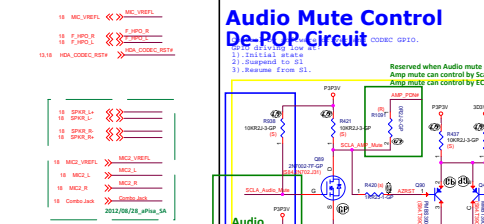
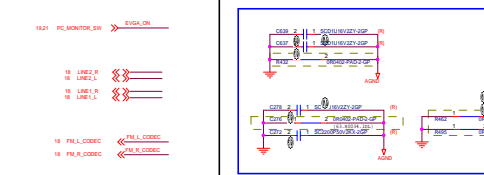
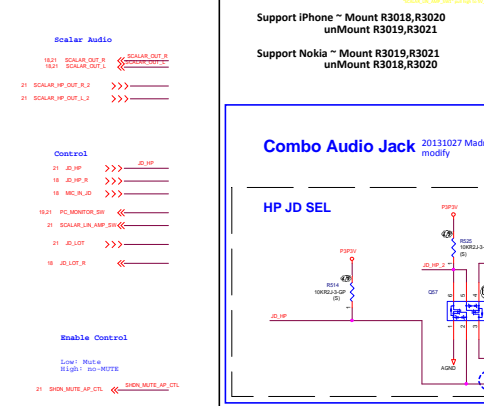
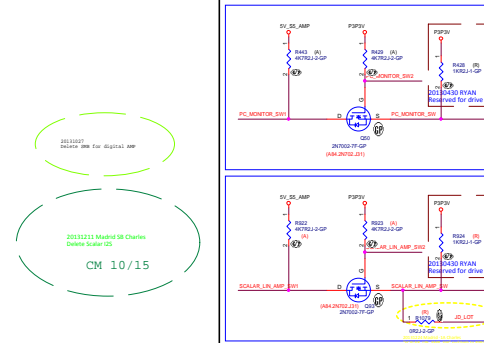
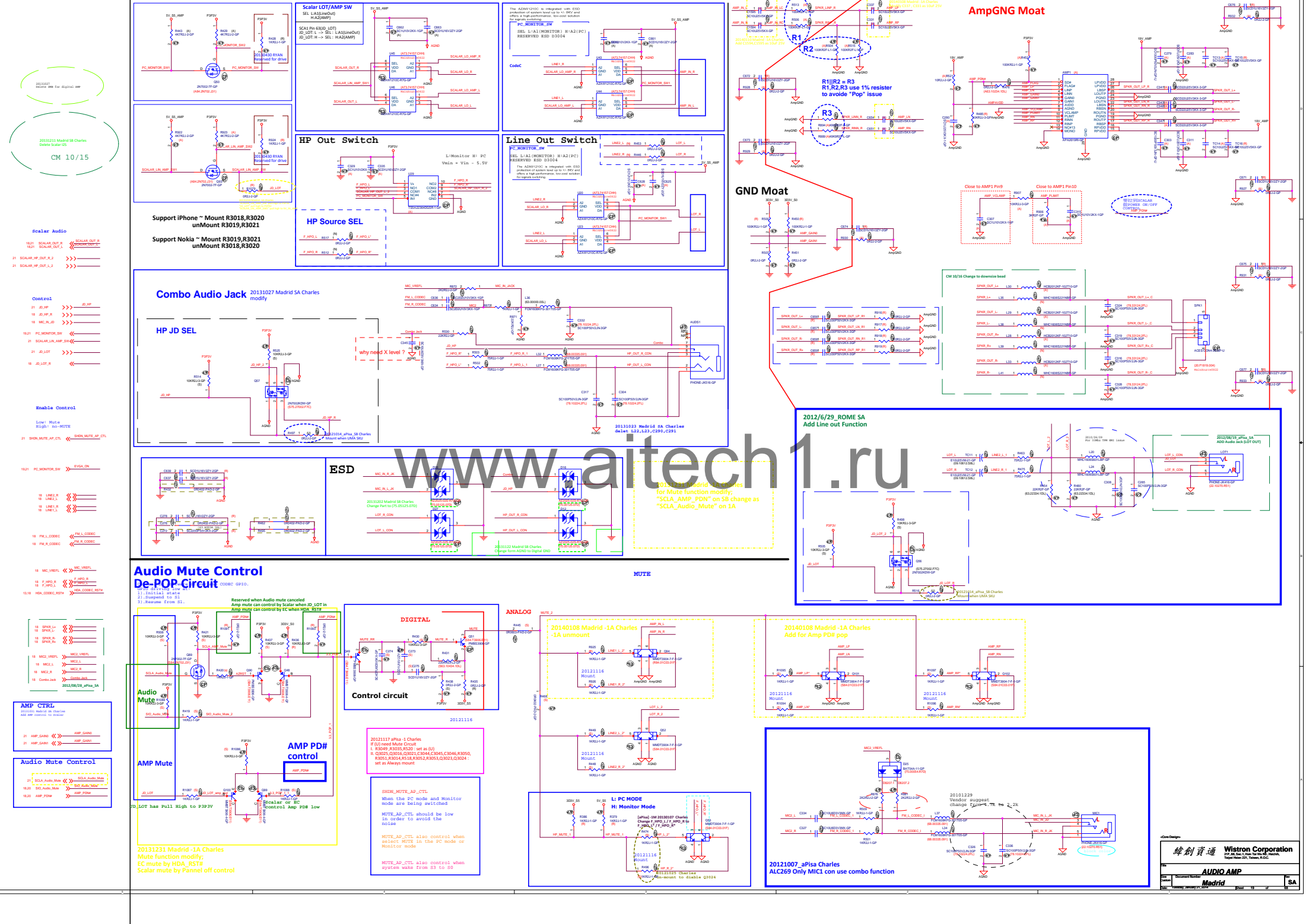
Real Line in

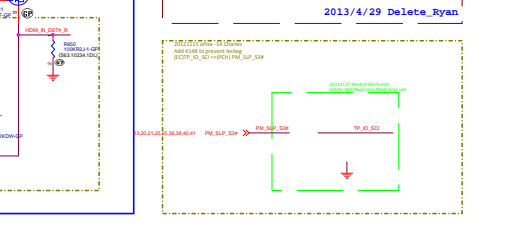
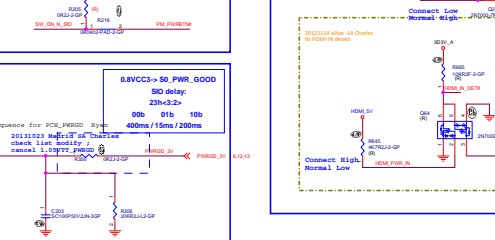
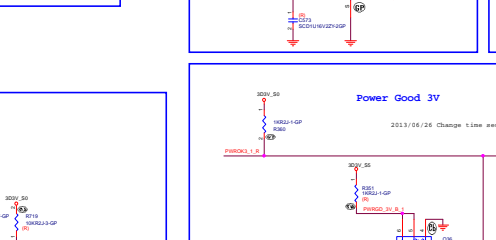
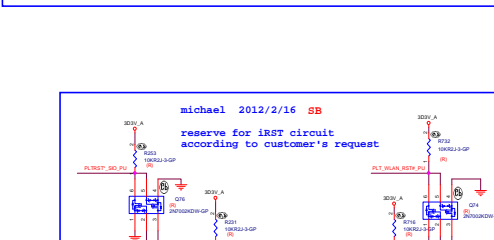
Real Line Out

20121007 aPisa Charles
Only MIC1 can use combo function

20131122 Madrid SB Charles
Add PCH BEEP to Codec

20111214 Follow Bremen design buzzer
20131010 Madrid Charles cancel BUZ





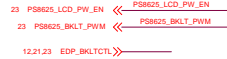
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80-83/96/95

If without use these pins, Please pull-up to 3.3V.
Don't let it floating
Pin19/24/25/30/48/57/71/75/77/80-83/96/95

SM Bus PH
SMB_DATA/CLK

	ID3
W/ Scalar	1
W/O Scalar	0

SSID = VIDEO



Mapping eDP-IN pin net
Colay the serial Capacity
eDP AUXIN C

```

21  DPD_LANE0N_C      >>> DPD_LANE0N_C
21  DPD_LANE0P_C      >>> DPD_LANE0P_C
21  DPD_LANE1N_C      >>> DPD_LANE1N_C
21  DPD_LANE1P_C      >>> DPD_LANE1P_C
21  DPD_HPD            >>> DPD_HPD

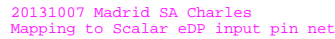
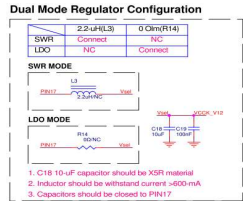
```

Colay power pin net
Difference Power source
Individual power Capacity

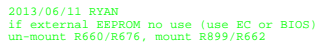
```

21 TMD5_3V3      >>> TMD5_3V3
    TMD5_3V3
    Replace
    P_3.3V_EDP_VDDIO

```



20131031 Madrid SA Charles
This two Bead must be (U)
to seperate 3D3V USB & P3P



		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2136 Supports three operation mode for system design.
Reserved 4.7K resistor pull up/low for mode selection

MODE CF

MODE CF

R16

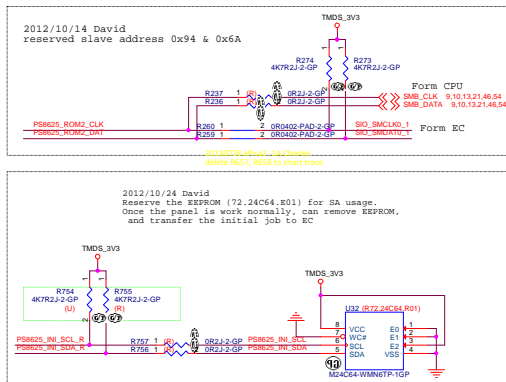
R17

ROM ONLY Mode : PIN47 4.7K pull low, PIN48 4.7K pull high

EP Mode : PIN47 4.7K pull high, PIN48 4.7K pull low

EEPROM Mode : PIN47 4.7K pull high, PIN48 4.7K pull high

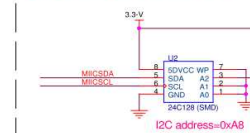
```
2013/06/11 RYAN
if external EEPROM no use (use EC or BIOS)
un-mount R660/R676, mount R899/R662
```



EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

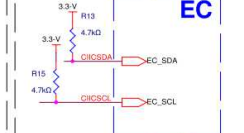
- 1- EEPROM with a size 8K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



I2C address=0xA8

EP Mode

External device connect to DP2LVDS by Pin13/Pin14, I2C protocol is used



«Core Design»

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Tainan, Taiwan, R.O.C.

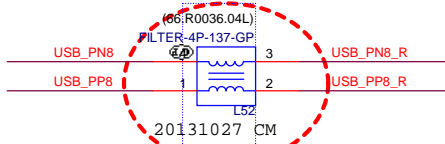
Title	RTD2136R eDP to LVDS
-------	-----------------------------

Size	Document Number	Rev
Custom	Madrid	SA
Date:	Tuesday, January 21, 2014	Sheet 22 of 58

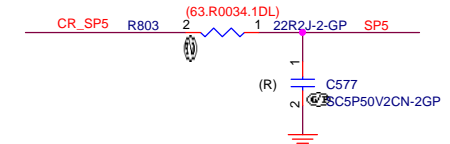
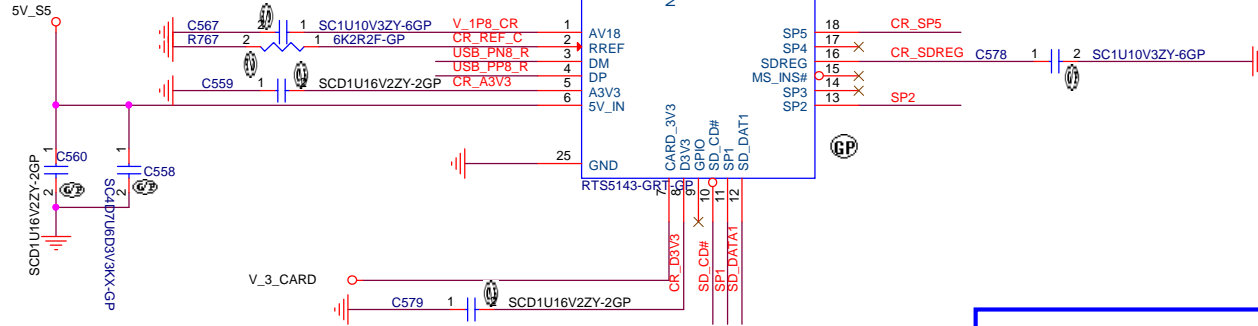
20131009 Madrid SA Charles
follow Florance
modify USB port follow Superb

11 USB_PN8
11 USB_PP8

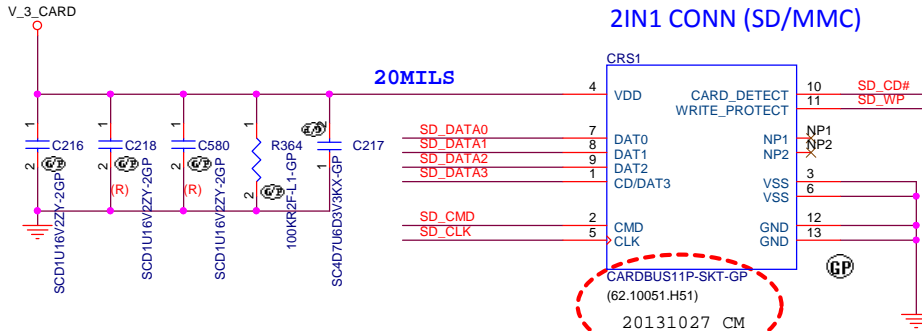
(MS / SD / MMC)



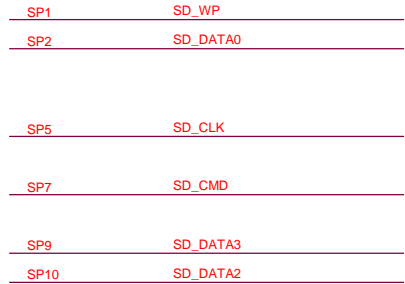
20131028 Madrid SA Charles ;
Swap



20130910 Ryan



2IN1 (SD/MMC) Combo Net



<Variant Name>

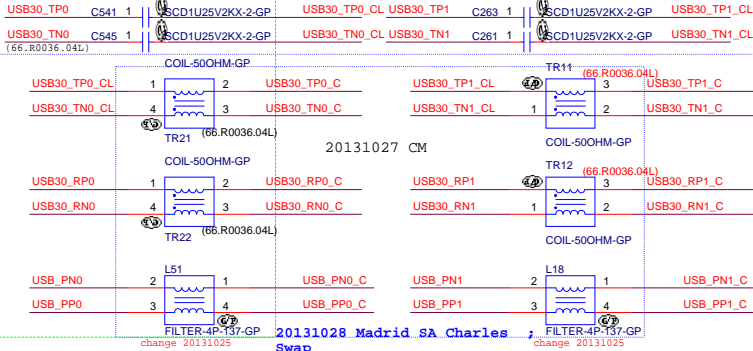
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RTS5143 (CARD READER)
Size B Document Number
Madrid
Date: Tuesday, January 21, 2014 Sheet 24 of 68
Rev SA

EMI_USB

20131016 Madrid SA charles
modify

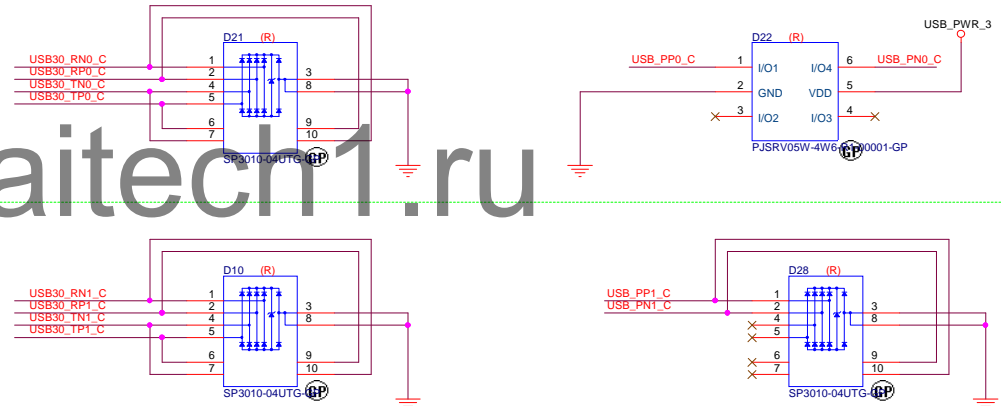
change 20131025



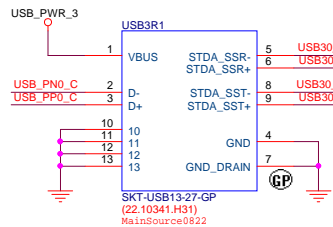
20131121 Madrid SB Charles
Modify the USB2R1 as USB3R1

ESD_USB

20131121 Madrid SB Charles
Modify the USB2R1 as USB3R1

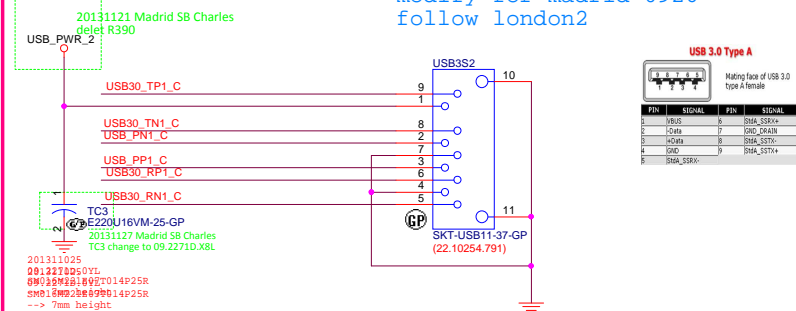


REAR USB3.0



Side IO USB3 connector

modify for madrid 0926
follow london2



USB Power Arrangement

USB_PWR_1:USB3S1+USBRF1 = 1400mA (原USB30_VCCA)

USB_PWR_2:SD+ USB3S2 + USB2R3 = 1900mA

USB_PWR_3: USB2R2+USB2R1+Touch = 1400mA

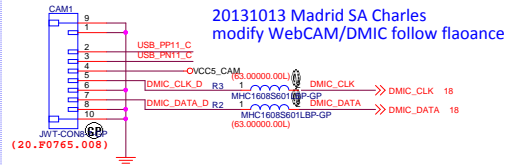
Title			
<Title>			
Size	Document Number		
Customer	Madrid		
	Rev SA		
Date:	Tuesday, January 21, 2014	Sheet	26 of 68

SSID =USB2.0

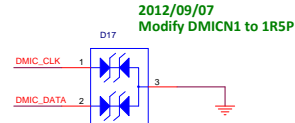
Pair	Device
0	USB3.0 Ext. port 1 (Side)
1	USB3.0 Ext. port 2 (Side)
2	Real USB2.0 ()
3	Real USB2.0 ()
4	Real USB2.0 ()
5	RF USB2.0 (Dual)
6	X
7	X
8	CR
9	Wireless LAN+BT
10	Touch
11	Webcam
12	X
13	X

20131121 Madrid SB delet USB_PN2/PP2
 11 USB_PN6
 11 USB_PP3
 11 USB_PN4
 11 USB_PP4
 11 USB_PN5
 11 USB_PP5
 11 USB_PN10
 11 USB_PP10
 11 USB_PN11
 11 USB_PP11
 11 USB_OC_23_N
 11 USB_OC_45_N

WEB CAM [USB Port11]



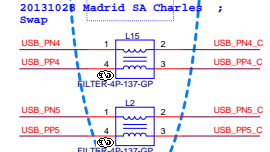
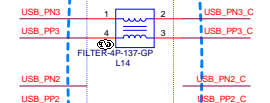
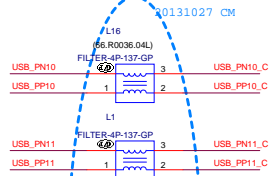
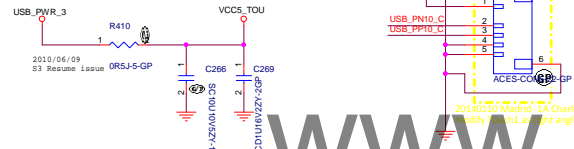
DMIC Connector



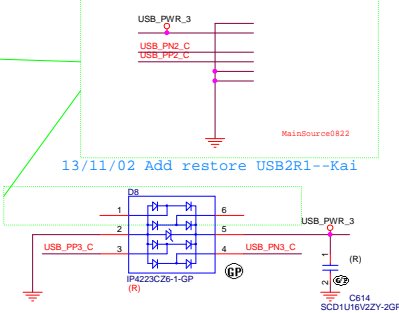
20131013 Madrid SA Charles
Delete DMIC1

TOUCH Connector

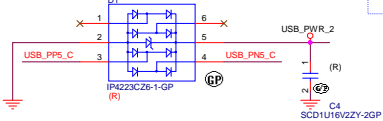
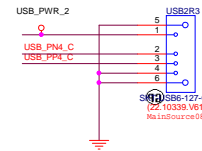
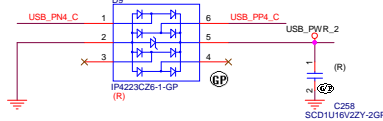
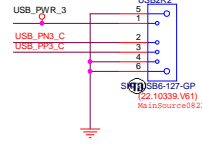
Share USB20 Pwr SW3



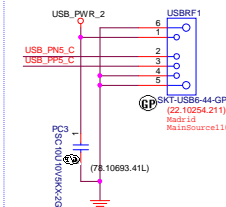
20131121 Madrid SB Charles
delet the USB2R1 Modify to USB3R1



REAR USB2.0



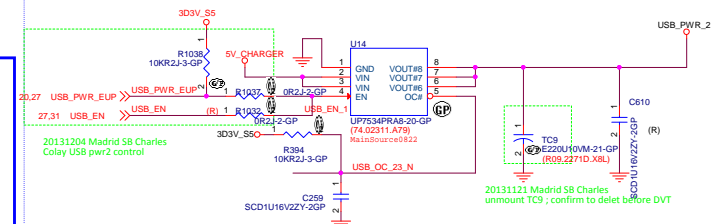
RF Dongle USB2.0



20131027 Madrid SA Charles
USB Power Arrangement
 USB_PWR_1:USB3S1+USBRF1 = 1400mA (原USB30_VCCA)
 USB_PWR_2:SD+ USB3S2 + USB2R3 = 1900mA
 USB_PWR_3: USB2R2+USB2R1+Touch = 1400mA
 VCC5_USB_23; VCC5_USB_45

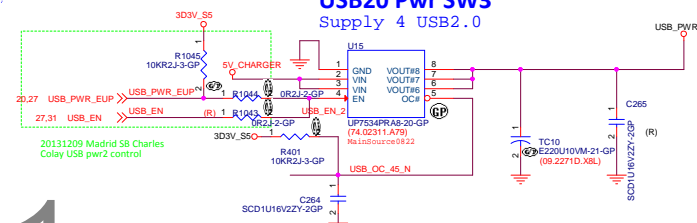
USB20 Pwr SW1

USB20 Pwr SW2



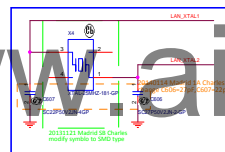
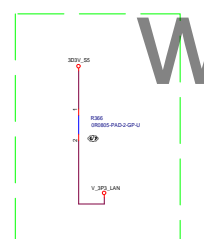
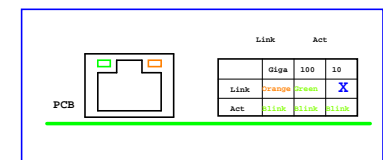
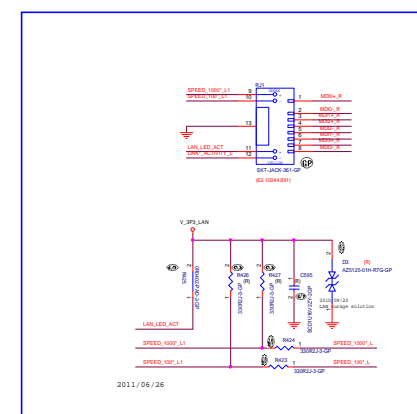
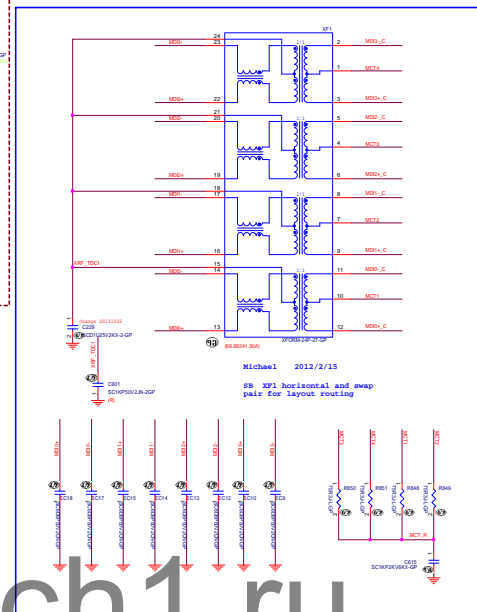
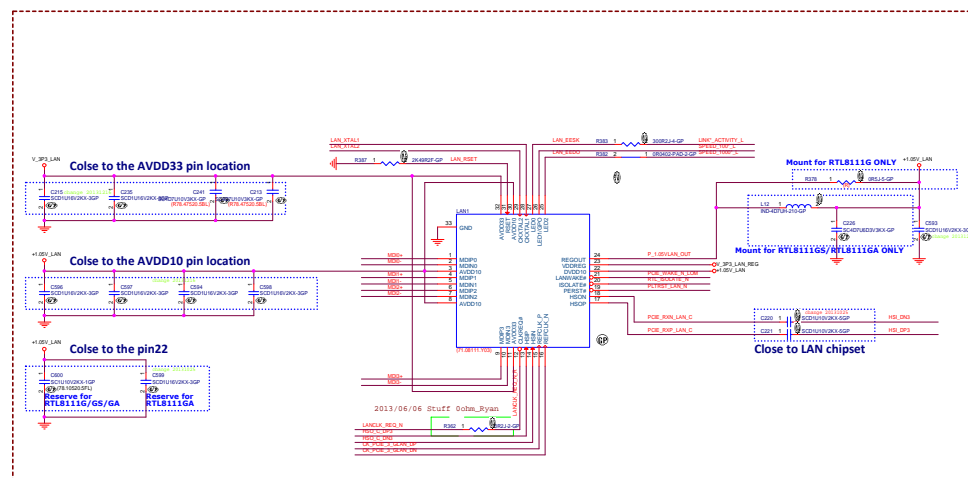
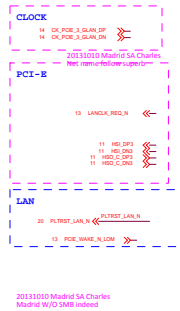
USB20 Pwr SW3

Supply 4 USB2.0

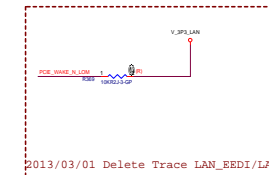
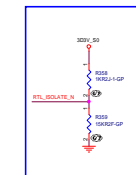
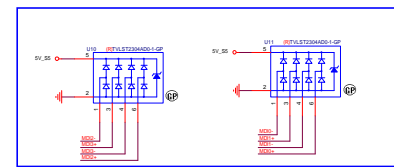
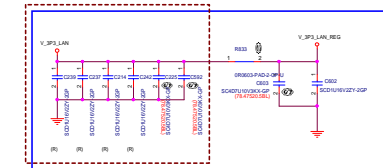
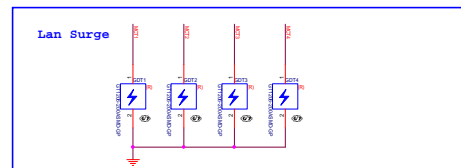


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Title: Rear USB/TOU/Dongle/Web Cam
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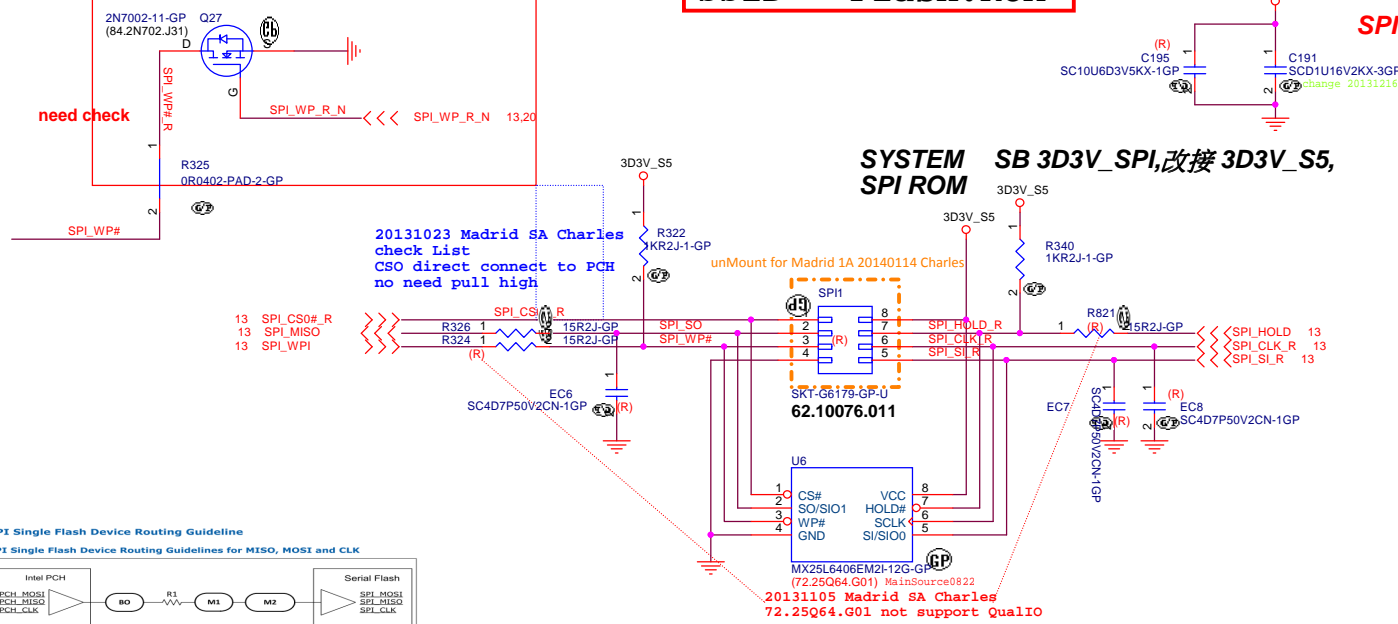
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SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil
SPI ROM Equal length need to less than 500mil

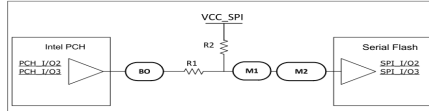


22.3.1.1 SPI Single Flash Device Routing Guideline

Figure 22-2. SPI Single Flash Device Routing Guidelines for MISO, MOSI and CLK



Figure 22-3. SPI Single Flash Device Routing Guidelines for I/O2 and I/O3



Note: I/O2 and I/O3 connection has to be pulled up with 1k ohm

Figure 22-4. SPI Single Flash Device Routing Guidelines for CS0#

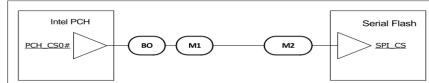
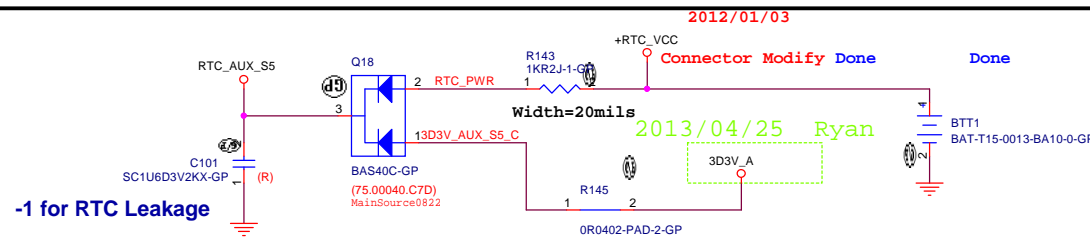


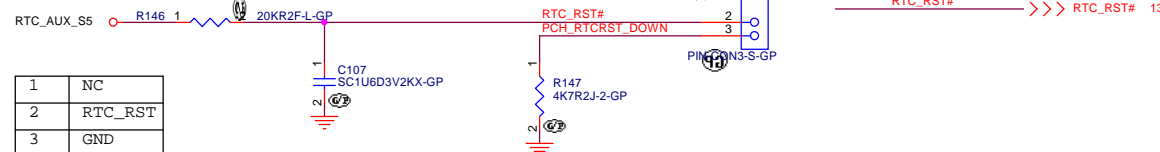
Table 22-3. SPI Single Flash Device Routing Guidelines (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Breakout Trace Length	BO	MS,SL	inch	<1"
Length 1	M1	MS,SL	inch	1"-5"
Length 2	M2	MS,SL	inch	0.5"-1"
Total length	BO, M1, M2	MS,SL	inch	1.5" - 7"
Resistor	R1		ohm	15
Resistor	R2		ohm	1k

SSID = RBATT



Clear CMOS

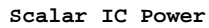



2011/9/30

Add CLR CMOS circuit

<Core Design>

AO3418 NMOS 3.1A, 60mohm,Vgs=10V **Michael 2011/12/01**
NMOS H: Enable L:Disable **change 5V_S5 to 5V_Charger**
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)



GPI input		From	High	Low	Default
Pin69	GPI-1 PC Power ON  PM_SLP_S3M 13,20,21,22,35,36,38,40,41	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel OnOff	SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

Pin55	GPO-2 Panel On/OFF	SCALAR_VDD_EN 2123	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor	PC_MONITOR_SW 1921	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin101	GPO-5 Video	BLON_EN# 2123	Scalar	Disable	Enable	Disable
Pin72	GPO-6 Audio Mute	SHDN_MUTE_AP_CTL 21	Scalar	on-Mute	MUTE	MUTE

VCC5_USB



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

USB2.0 Power SW

Size	Custom
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Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

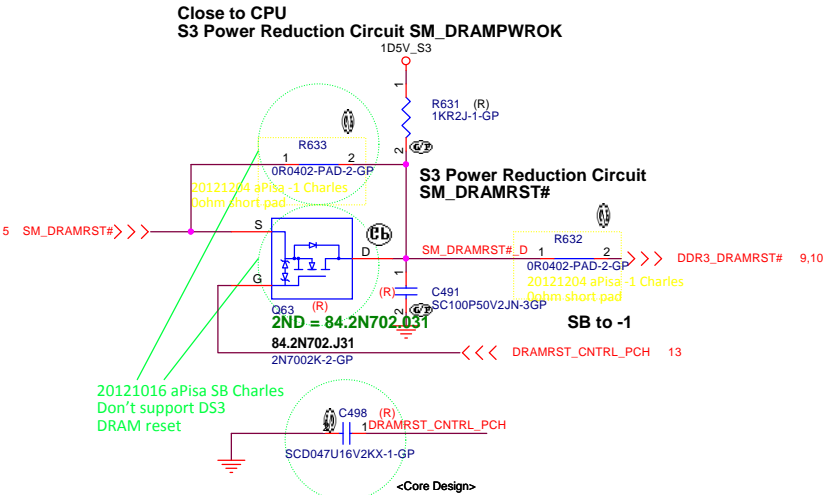
20121012 Jerry
Delete

5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

2013/03/11 Delete_Ryan

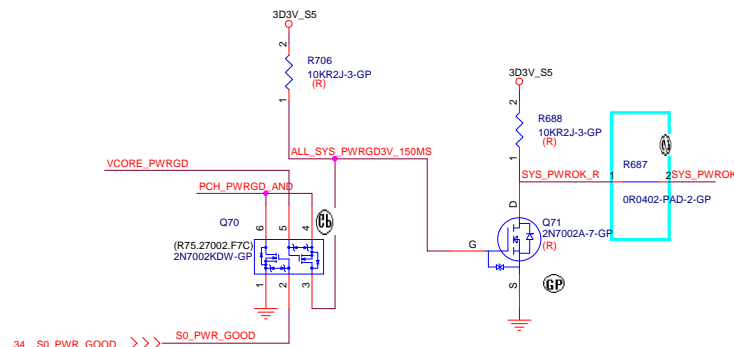
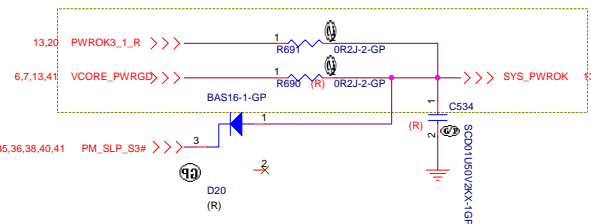
www.aitech1.ru

2013/03/05 NO USED_Ryan



Power Sequence

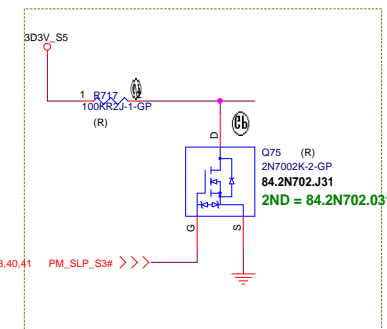
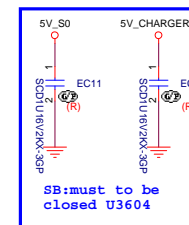
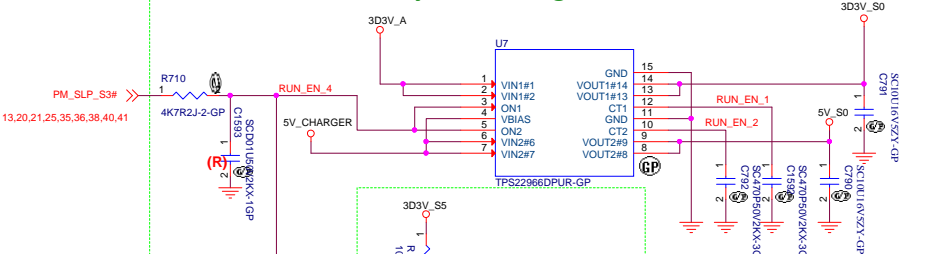
2013/06/26 Change time sequence for PCH_PWRGD Ryan



2011/9/22
Reserve for
system power
ok

ANNIE Run Power

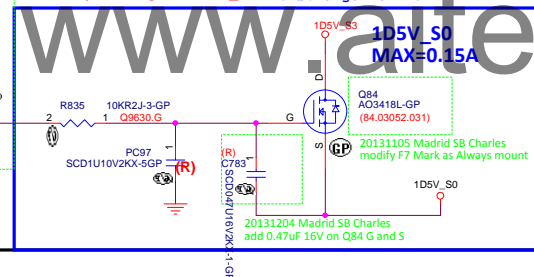
20131211 Madrid SB Charles
Modify 3V/5V Logic Control as Load Switch



20131018 Madrid SA Charles
Add to replace Page39 1D5V_S0

Add R3620 and R3621 for
discharge S5-->S0

1D5V_S0
MAX=0.15A



EUP Power

2012/06/08, ROME SA
Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

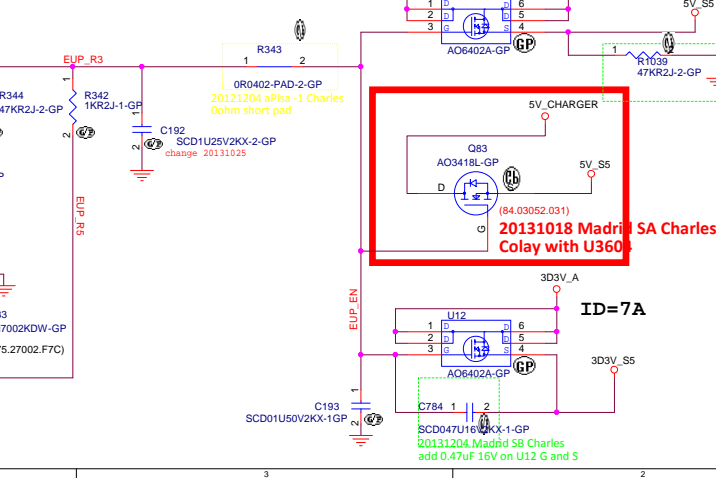
Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

Change R3608 from 47k to 33k

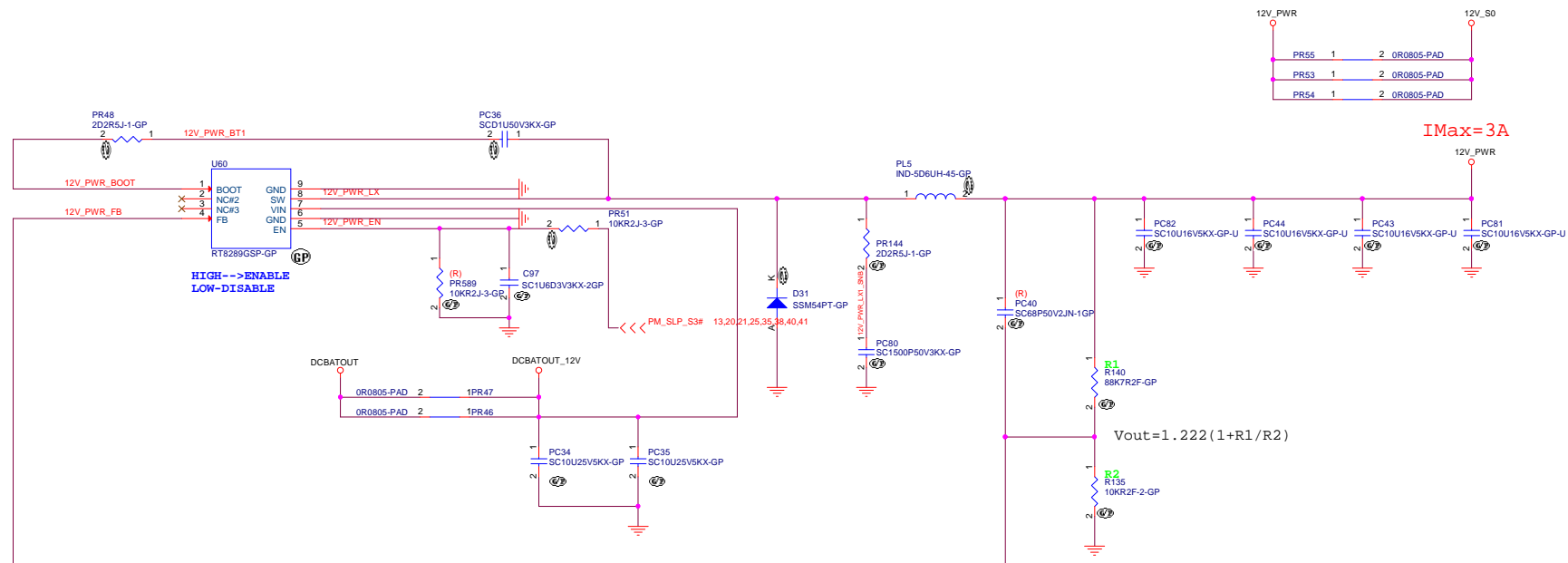


20131204 Madrid SB Charles
add 47K 63.47334.1DL for 5V_S5 for power discharge,
close to U39

20131018 Madrid SA Charles
Colay with U360

ID=7A

File		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Document Number		RUN POWER & SEQUENCE	
Custom		Madrid	
Date		Tuesday, January 21, 2014	
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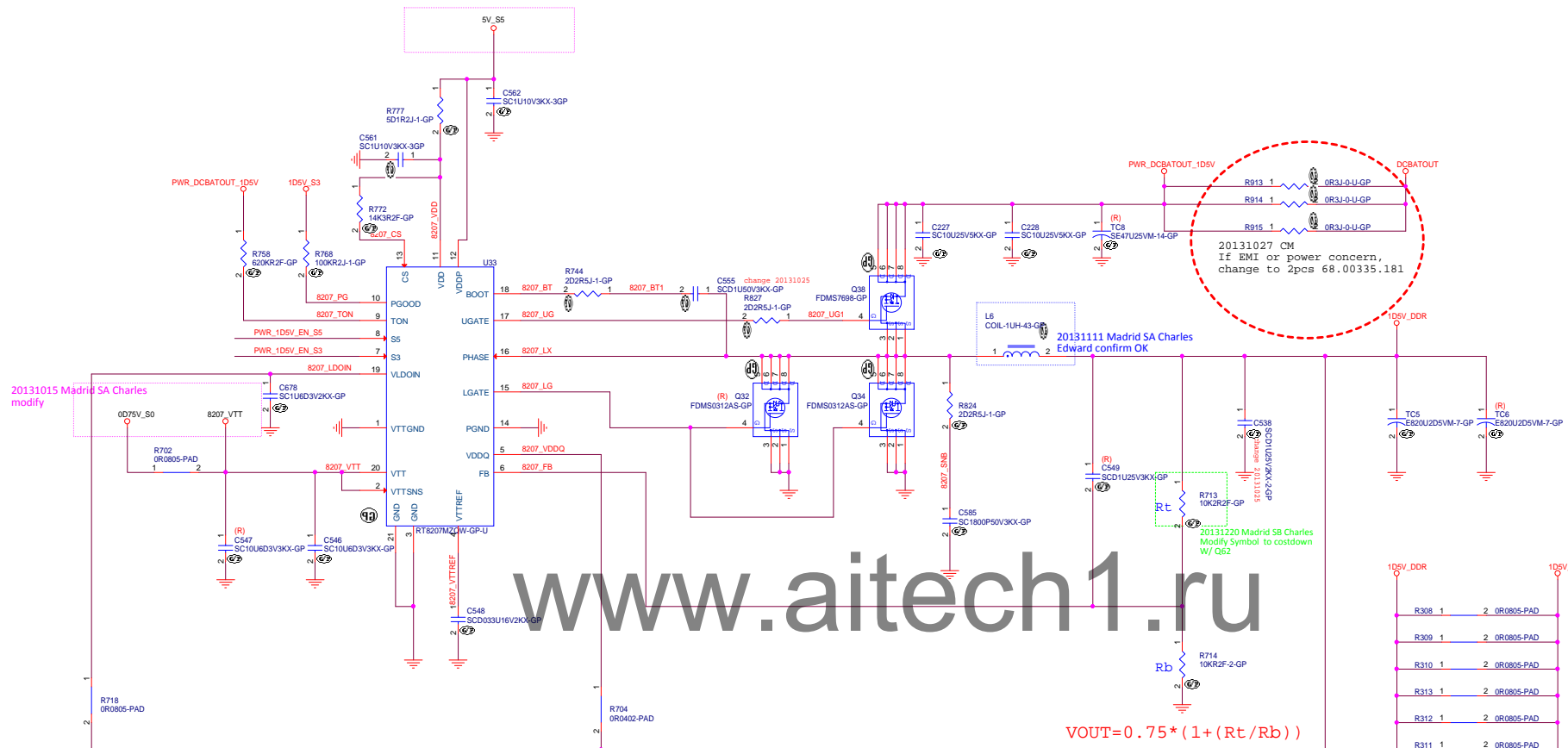
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<Core Design>

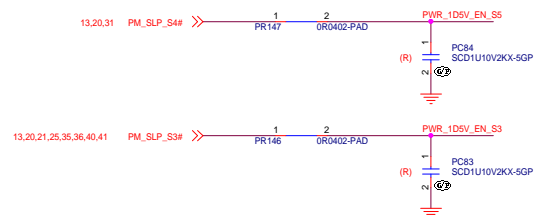
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 12V(NCP1589A)		Rev
Size	Document Number		SA
Custom			
Date:	Tuesday, January 21, 2014	Sheet 36 of 68	



ENABLE SIGNAL

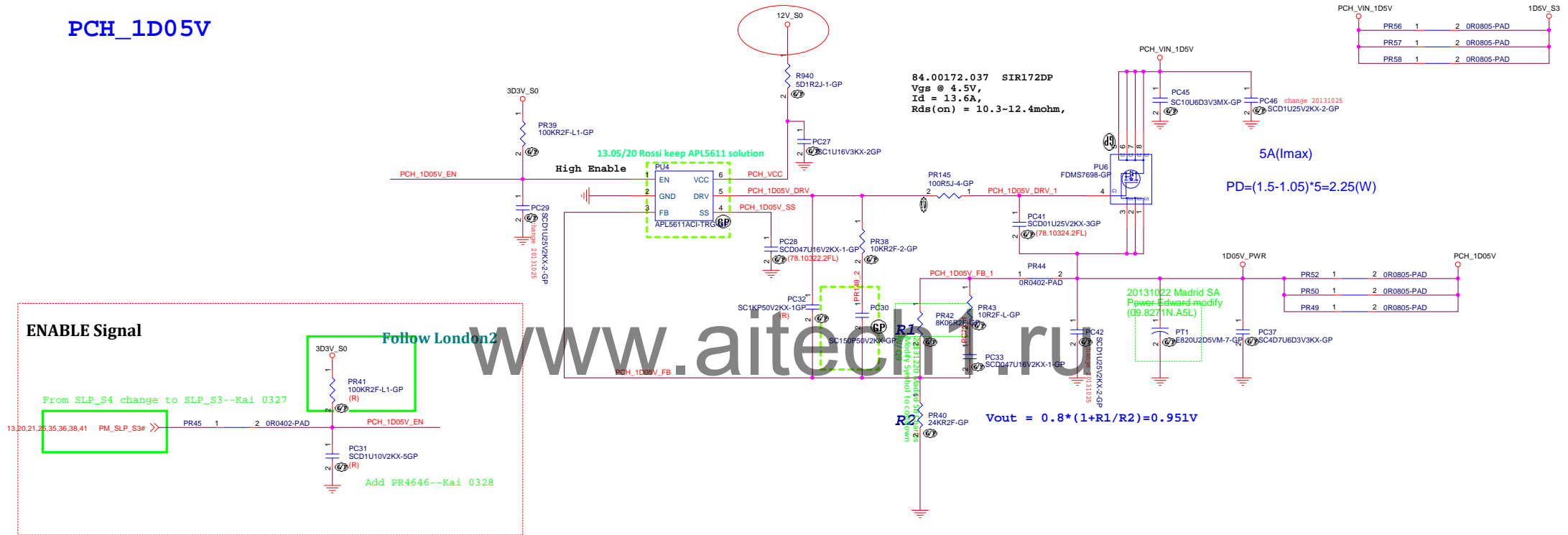


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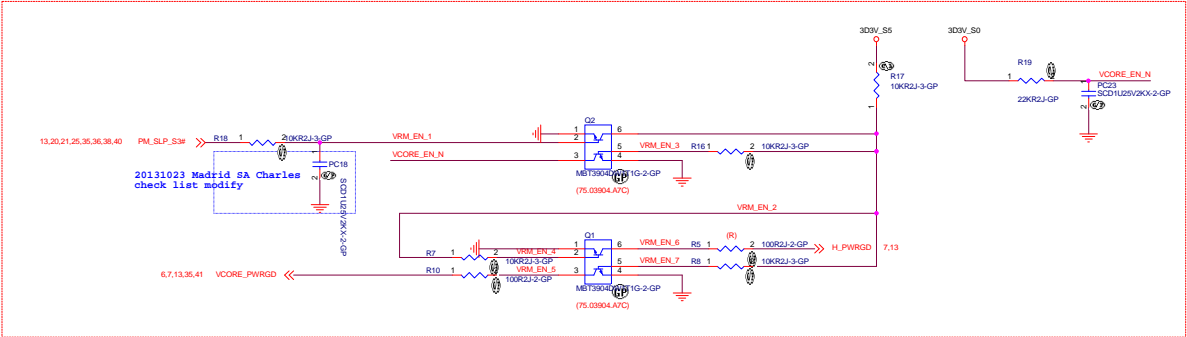
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DC to DC 1D5V(APL5930)			
Size	Document Number		Rev
B			SA
Date:	Tuesday, January 21, 2014	Sheet	39 of 68

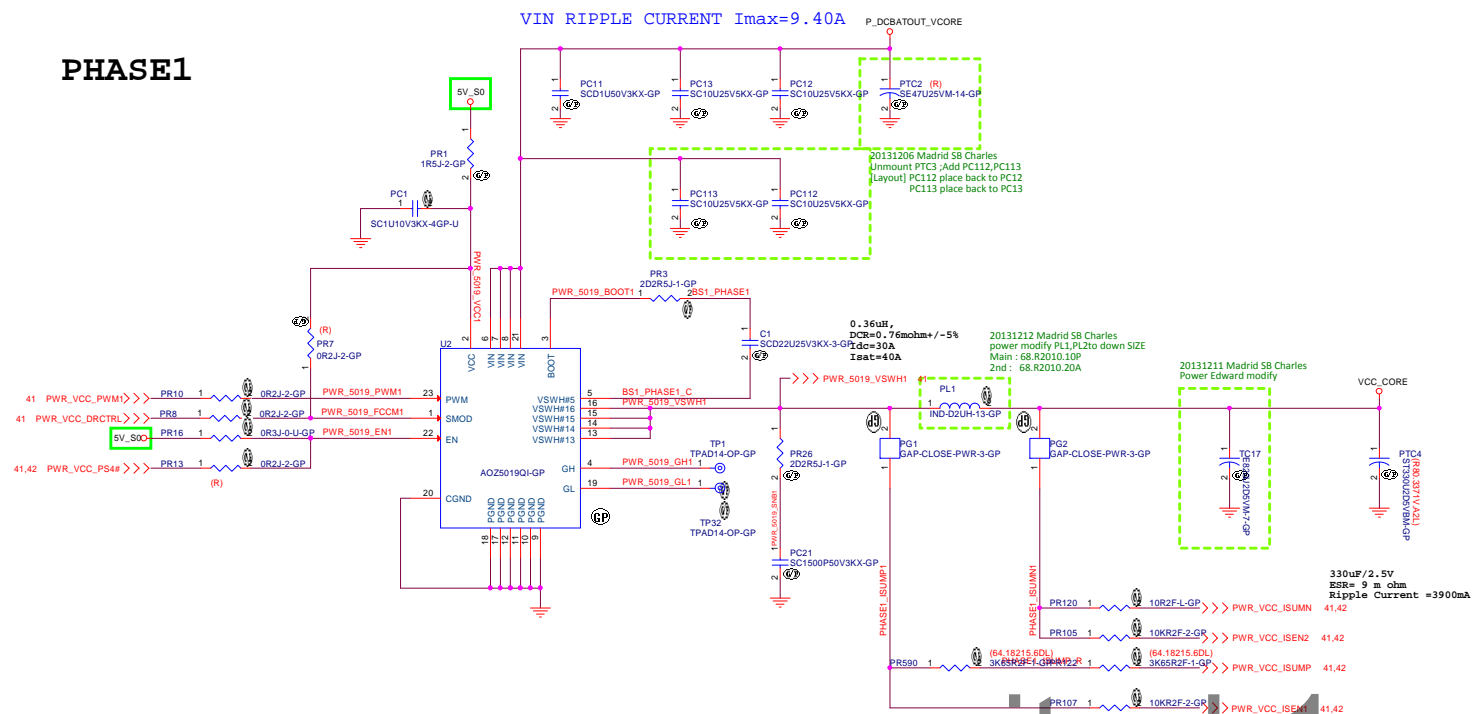
PCH_1D05V



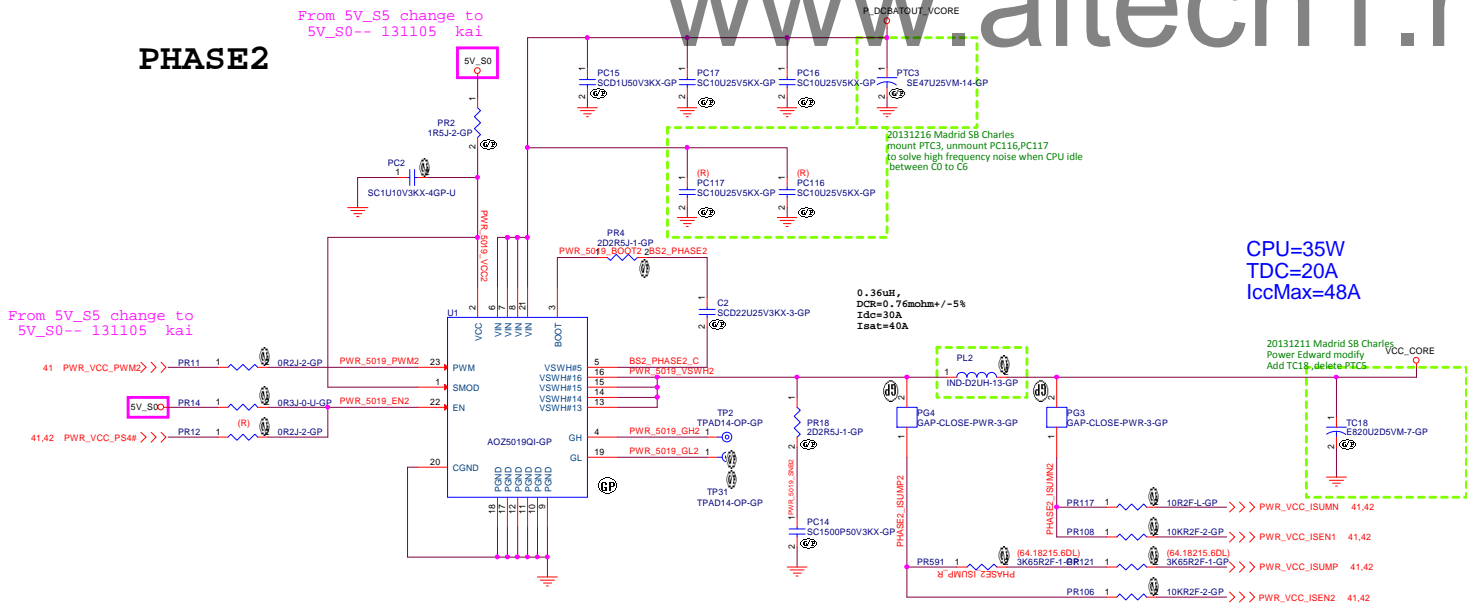
SSID = CPU.Regulator



PHASE1



PHASE2



<Core Design>

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title

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Size

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Date _____

CPUCORE_ISL95825(2/2)

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July 21, 2014

Rev

SA

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HDMI-IN

HDMI

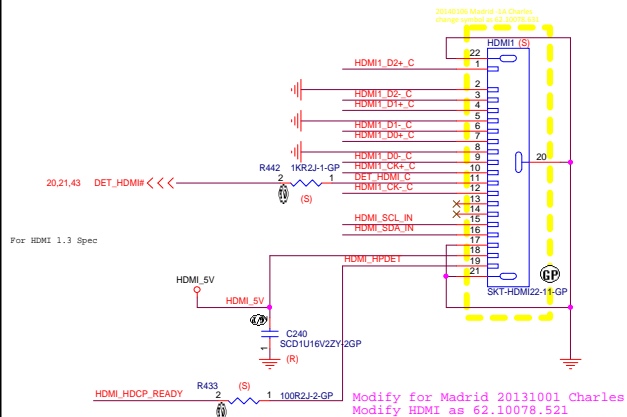
21,43 HDMI1_D2+ <<<
21,43 HDMI1_D2- <<<
21,43 HDMI1_D1+ <<<
21,43 HDMI1_D1- <<<
21,43 HDMI1_D0+ <<<
21,43 HDMI1_D0- <<<
21,43 HDMI1_CK+ <<<
21,43 HDMI1_CK- <<<

check!

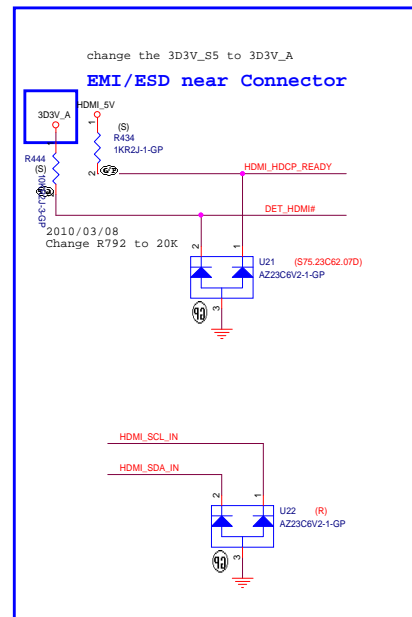
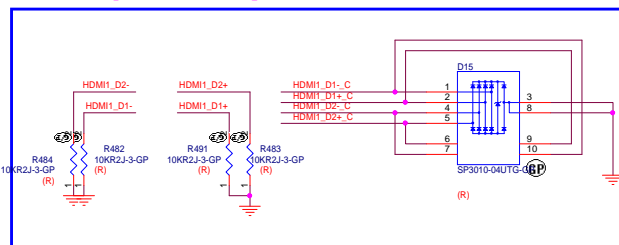
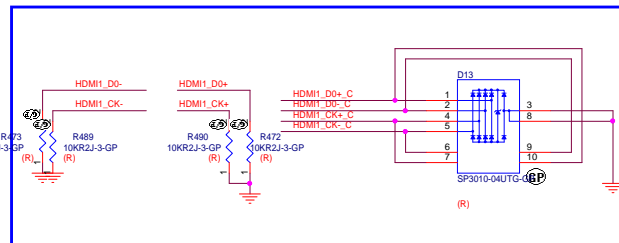
20,21,43 DET_HDMI# <<<
21 DDC_WP <<<
21,43 HDMI1_SDA <<<
21,43 HDMI1_SCL <<<
21 HDMI_HDCP_READY <<<

Use 62.10078.041 30u -> NG for production
-1A change to use 62.10078.291 and check
alternate source

Connector



EMI/ESD near Connector



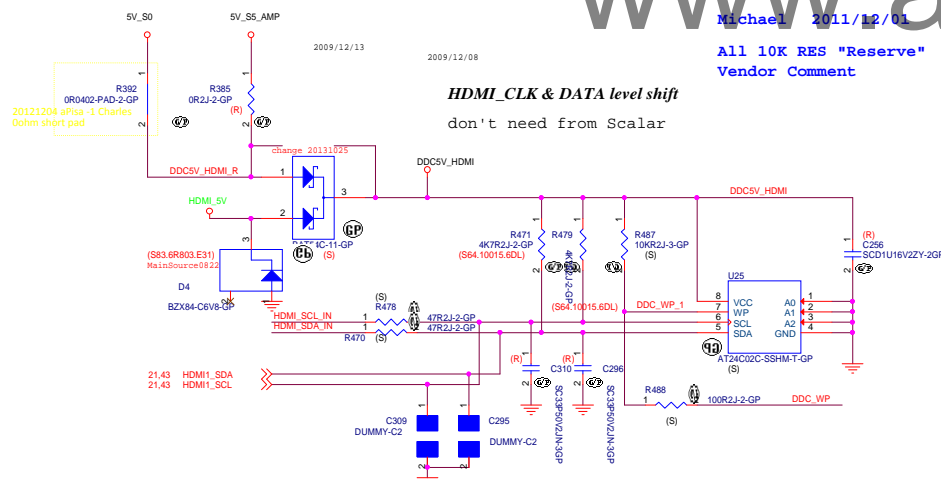
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Michael 2011/12/01

All 10K RES "Reserve"
Vendor Comment

HDMI_CLK & DATA level shift

don't need from Scalar



Michael 2011/12/01

change R283 and R305 from 100ohm to 47ohm

Vendor Comment

<Core Design>

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HDMI IN			
Size	Document Number	Rev	SA
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SSID = VIDEO

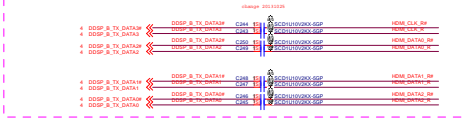
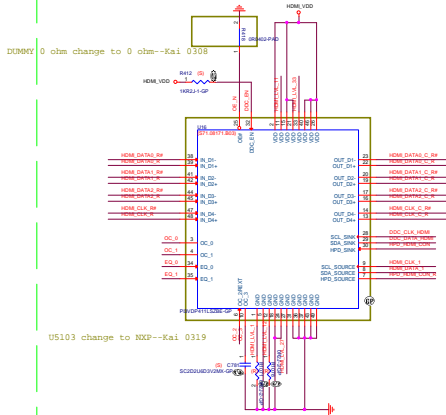
UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103-C5110 to 0 ohm resistor

	Pin 3	Pin 4	Pin 6	Pin 10	Pin 34	Pin 35
T1.03411.B03	Low	Low	Low	Low	Low	Low
T1.03411.D03	Low	Low	NC	NC	NC	NC
NOXP	Bq	NC	NC	NC	NC	NC

Eg : Check SPEC

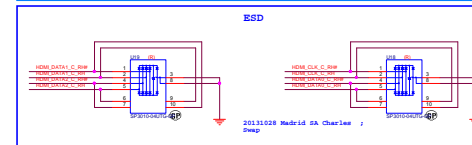
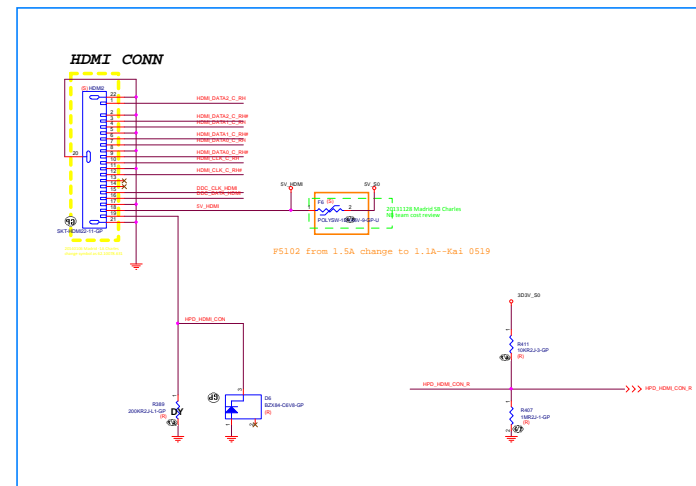
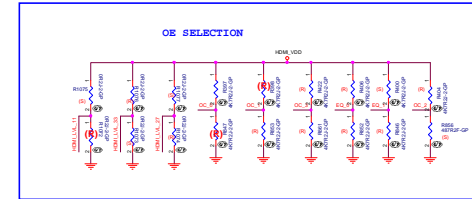
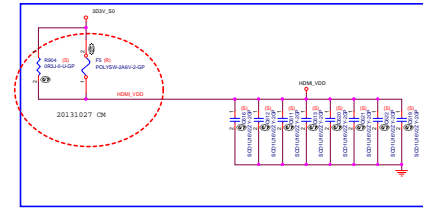
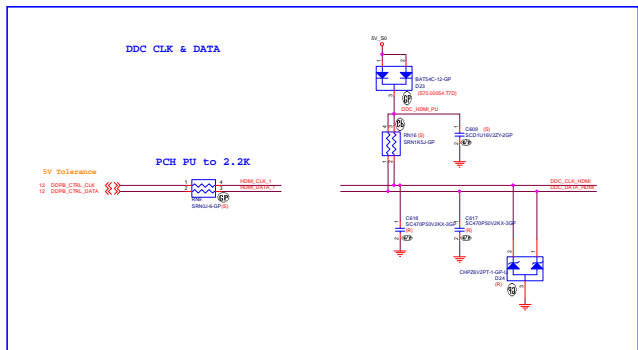
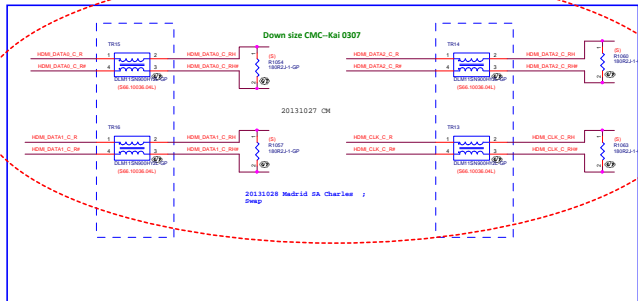
20131014 Madrid SA Charles

HDMI port0 & port2 cross

20131212 Madrid SB Charles
modify NWR/Parade Collet solutions

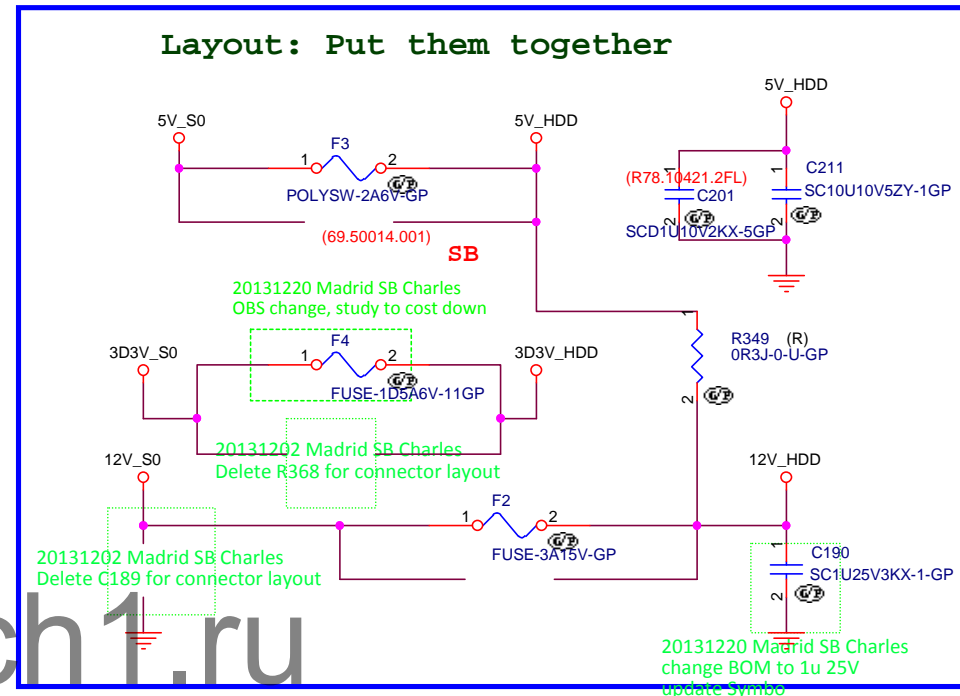
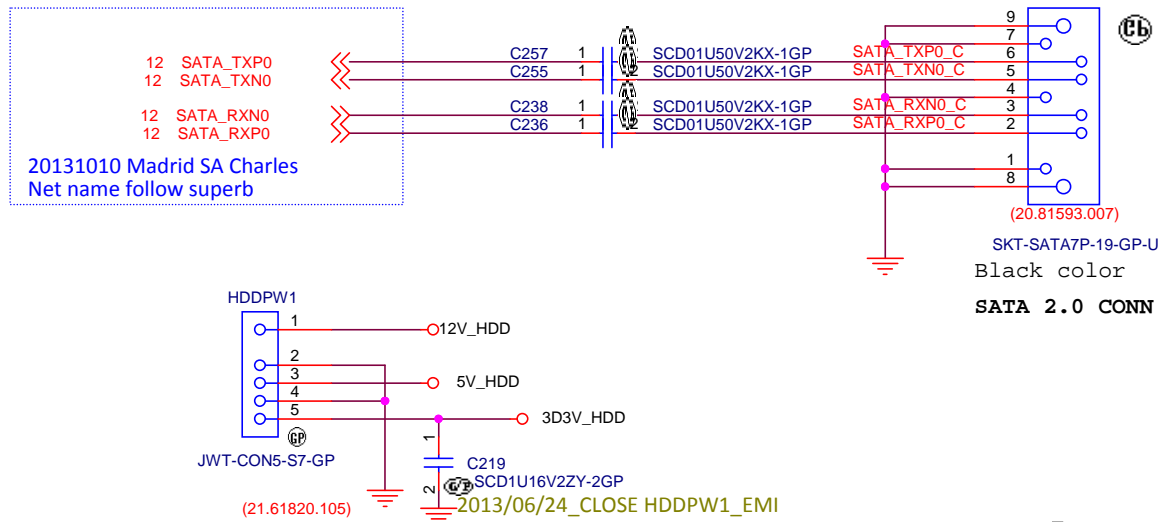
U5103 change to NXP--Kai 0319

Modify for Madrid 20131001 Charles
Modify HDMI as 62.10078.521

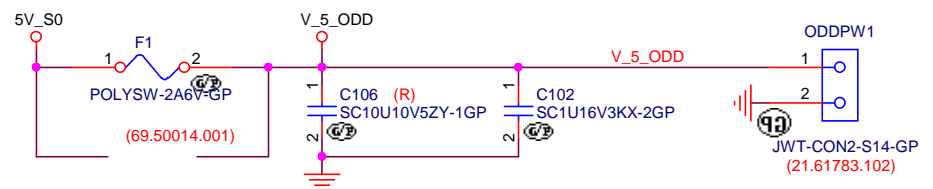
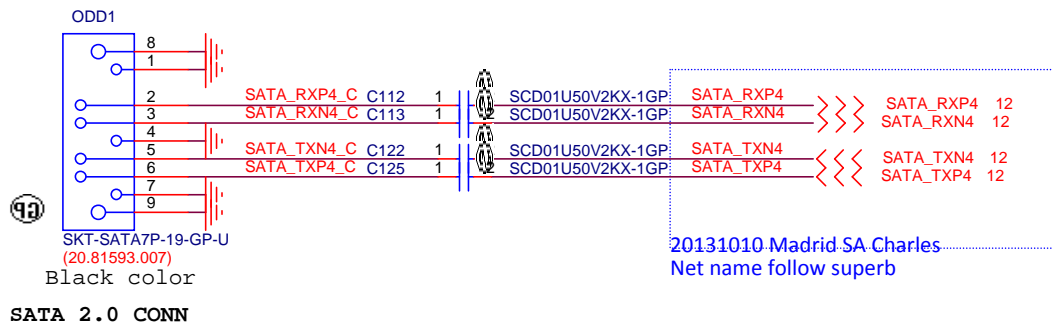


SSID = SATA

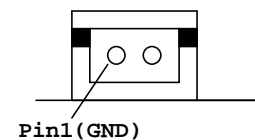
SATA HDD/Power Connector



SATA ODD/ Power Connector



Front View



20.60341.104: 4pin right angle
20.60334.103: 3pin right angle

<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/ODD			
Size	Document Number		Rev
Custom	Madrid		SA
Date:	Tuesday, January 21, 2014	Sheet 45	of 68

SSID = Wireless and Bluetooth

2011/11/29

Michael

ADD USB for BT Function

Mini Card Connector(Wireless LAN+BT)

2012/06/26_ROME SA Change symbol to 5.2mm

Michael 2011/11/29
Change 1D5V_MEM to 1D5V_S0

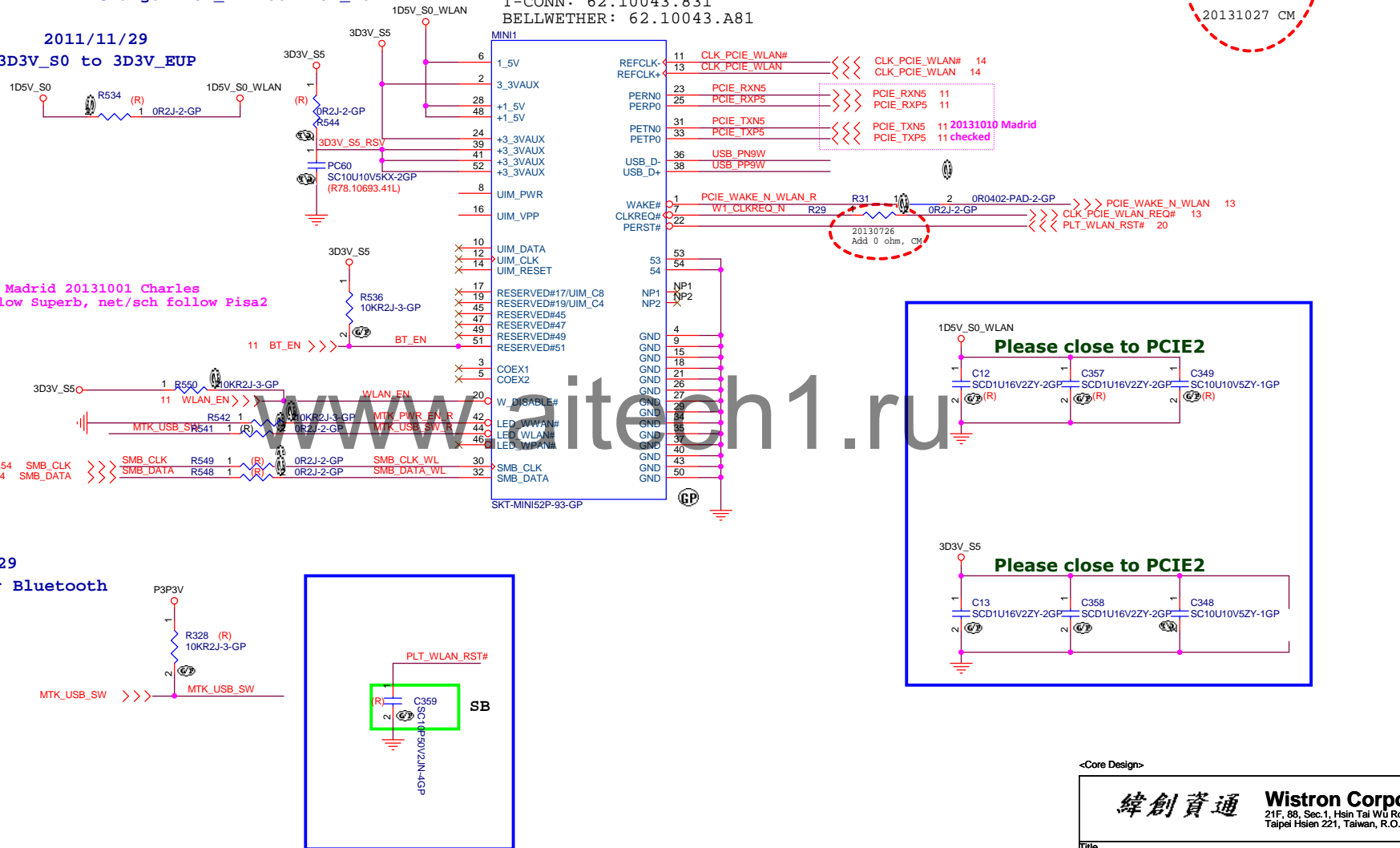
Height: 5.2mm
T-CONN: 62.10043.831
BELLWETHER: 62.10043.A81

Michael 2011/11/29
Change 3D3V_S0 to 3D3V_EUP

2013/05/07 ADD_Ryan

modify for Madrid 20131001 Charles
symbol follow Superb, net/sch follow Pisa2

Michael 2011/11/29
Add W3_DISABLE_N for Bluetooth
Add R1091 and R1089



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Mini PCIE Card WLAN / BT
Size	Document Number	Rev	SA
Custom	Madrid		
Date:	Tuesday, January 21, 2014	Sheet	46 of 68

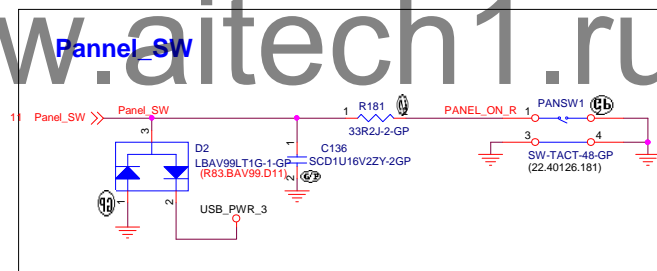
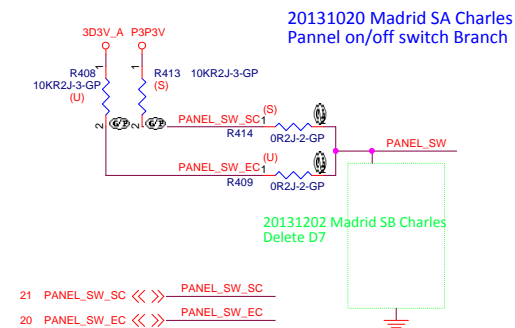
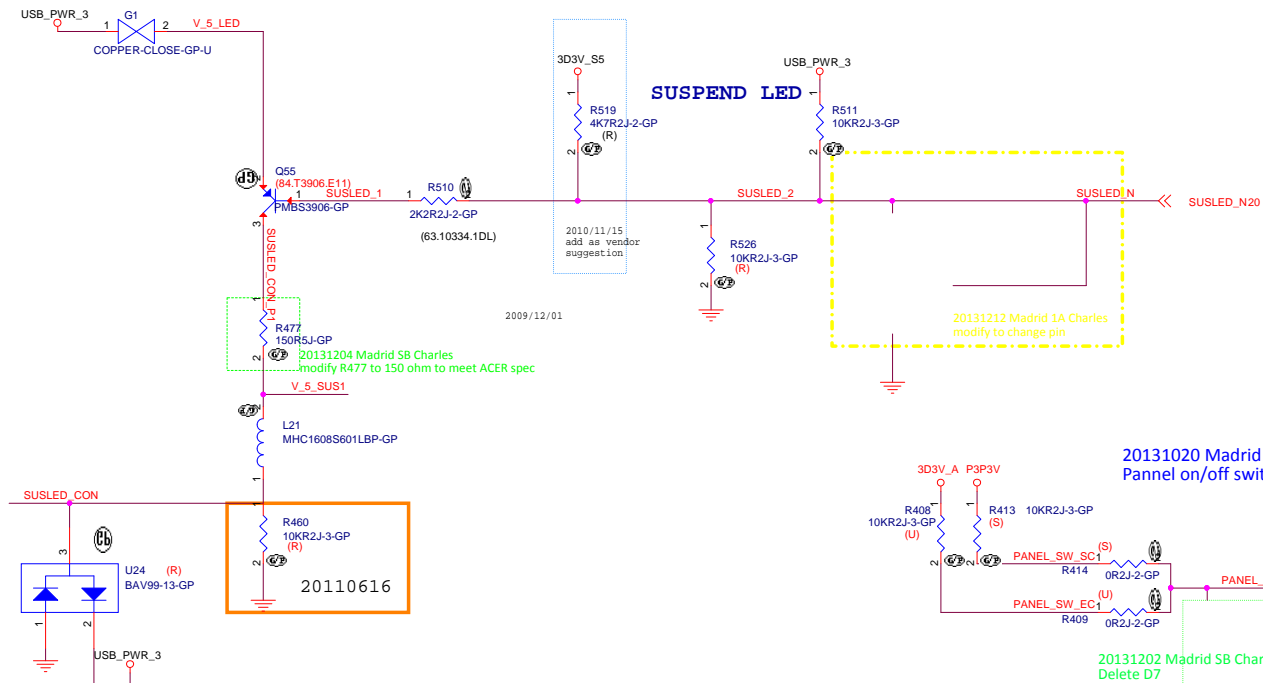
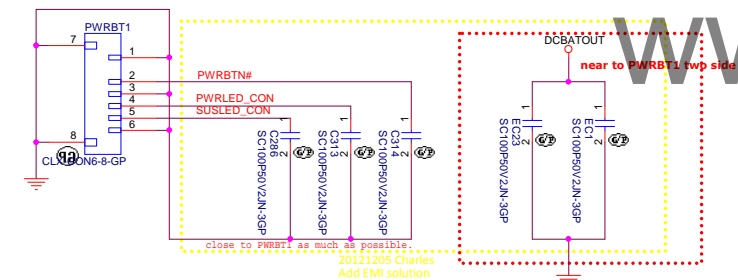
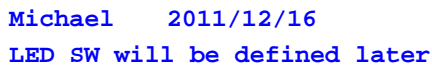
www.aitech1.ru

<Core Design>			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Mini PCIE Card (TV & SIM)			
Size	Document Number		Rev
Custom	Madrid		SA
Date:	Tuesday, January 21, 2014	Sheet 47 of	68

www.aitech1.ru

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Mini PCIE Card mSATA			
Size	Document Number		Rev
Custom	Madrid		SA
Date:	Tuesday, January 21, 2014		Sheet 48 of 68



<Core Design>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PWR BT/Side Key/LED			
Size Custom	Document Number	Rev	
Madrid		SA	
Date:	tuesday, January 21, 2014	Sheet	49 of 68

PWRLED_CON



2012/09/07_aPisa_SA
Add TPM Header

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緯創資通

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Debug connector

Document Number

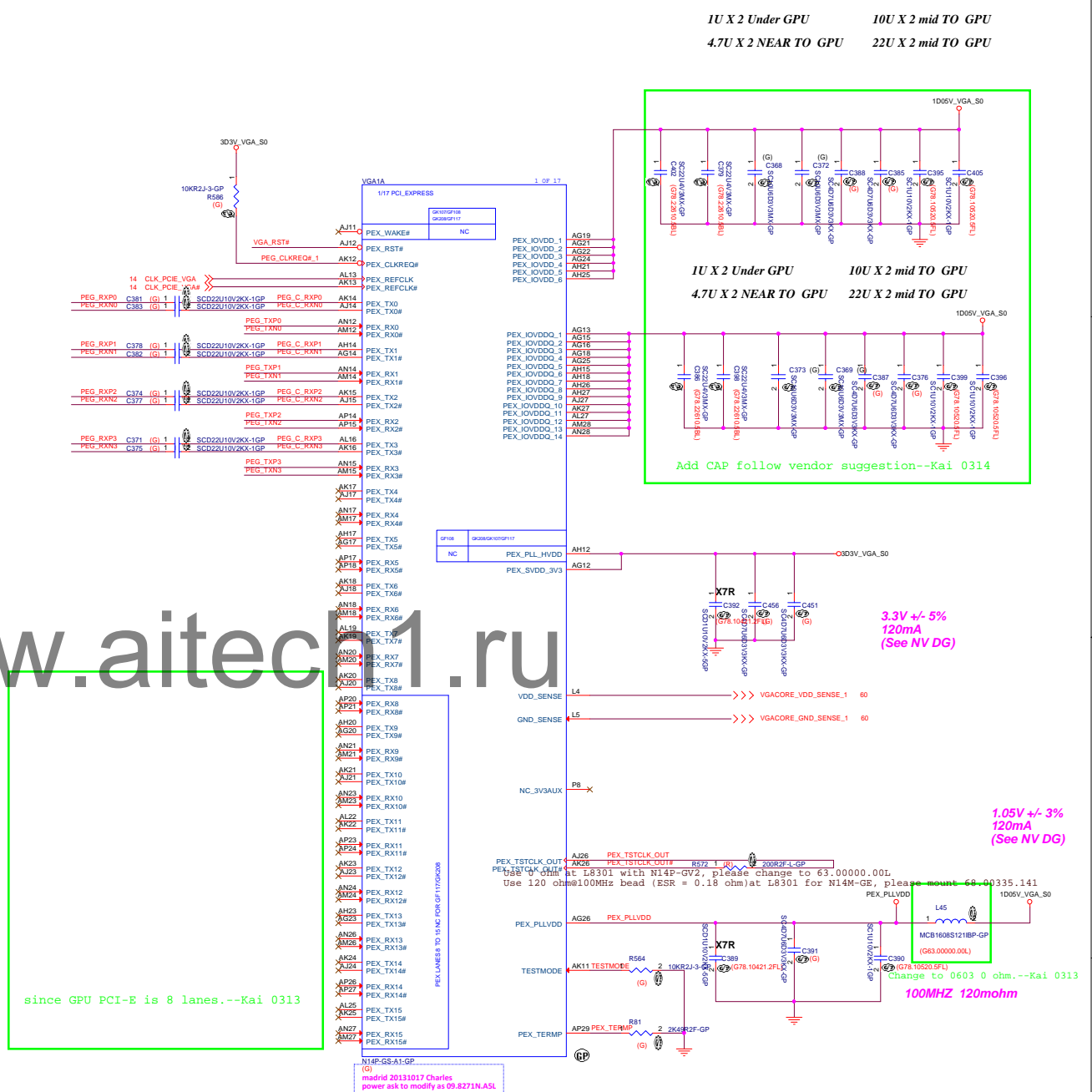
Madrid

Rev
S

Date: Tuesday, January 21, 2014

Sheet 50 of 68


```
reserve an active driver for PEX_RST#--Kai 0313
```

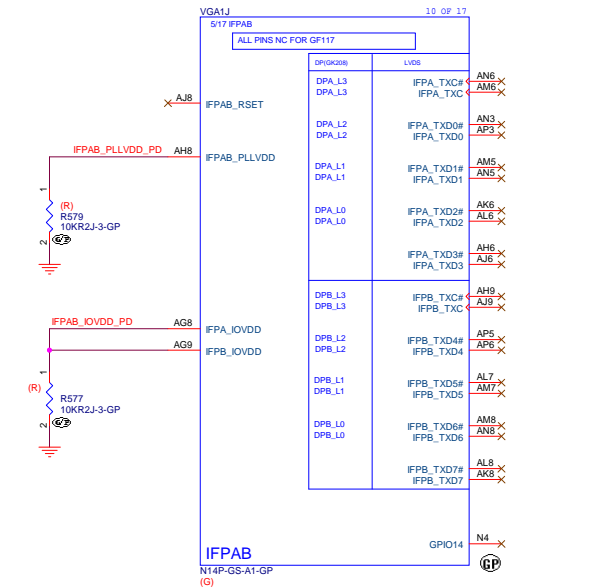


◀Core Design▶

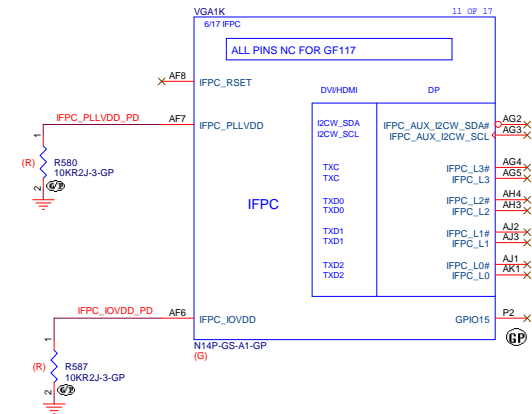
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
GPU (1/5): PEG			
Size A2	Document Number		Rev
	Madrid		SA
Date:	Tuesday, January 21, 2014		Sheet 51 of 68

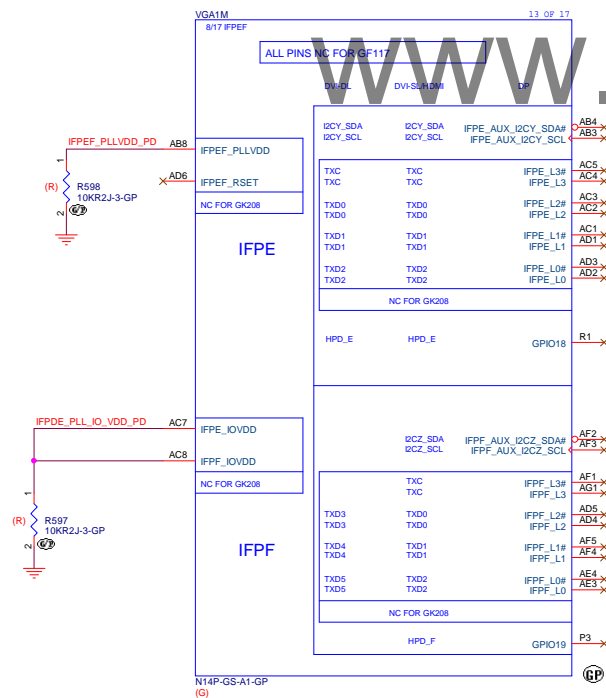
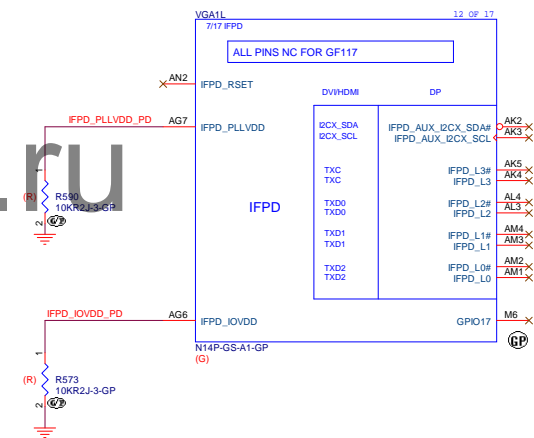
LVDS Interface

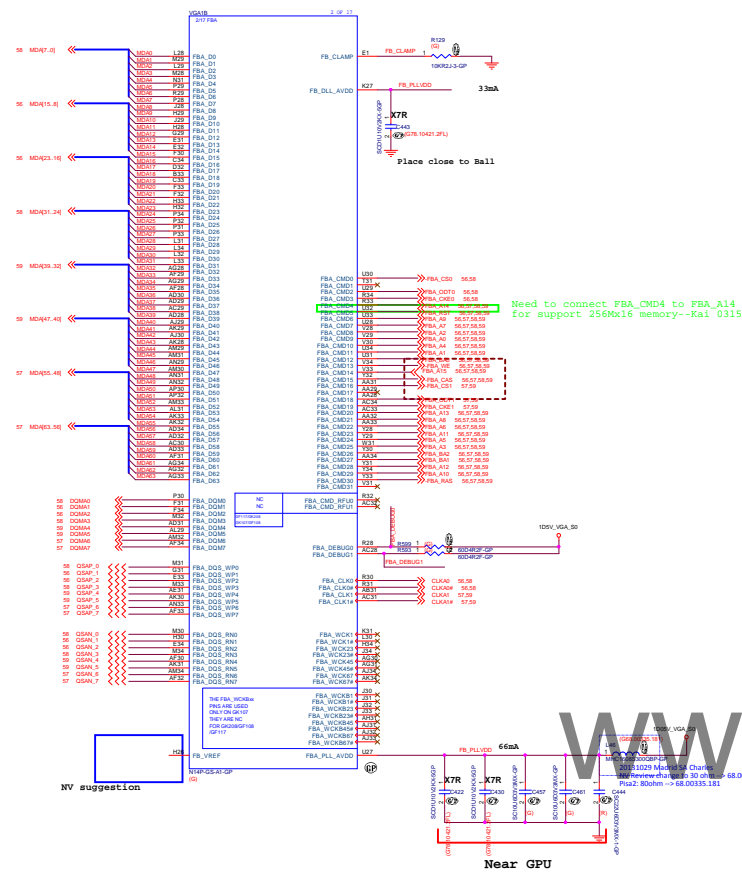


HDMI Interface

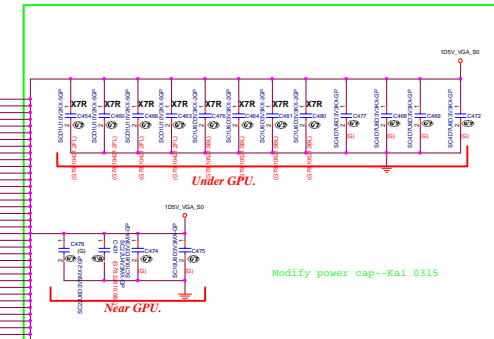
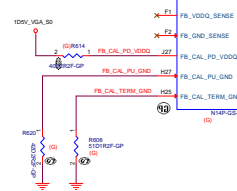
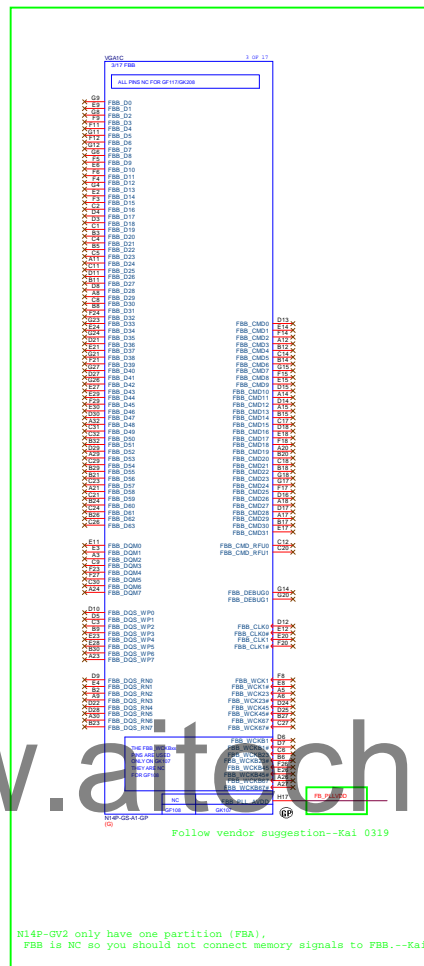
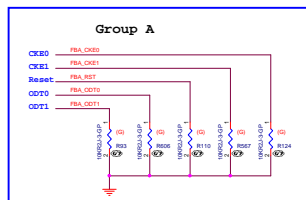


EDP Interface





FBCLK Termination place on VRAM side



EDP 50A (TDP 37W)

VGA CORE

VGA1H 8 OF 17

1517 NVDD

VDD_1

VDD_2

VDD_3

VDD_4

VDD_5

VDD_6

VDD_7

VDD_8

VDD_9

VDD_10

VDD_11

VDD_12

VDD_13

VDD_14

VDD_15

VDD_16

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VDD_253

VDD_254

VDD_255

VDD_256

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VDD_259

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VDD_272

VDD_273

VDD_274

VDD_275

VDD_276

VDD_277

VDD_278

VDD_279

VDD_280

VDD_281

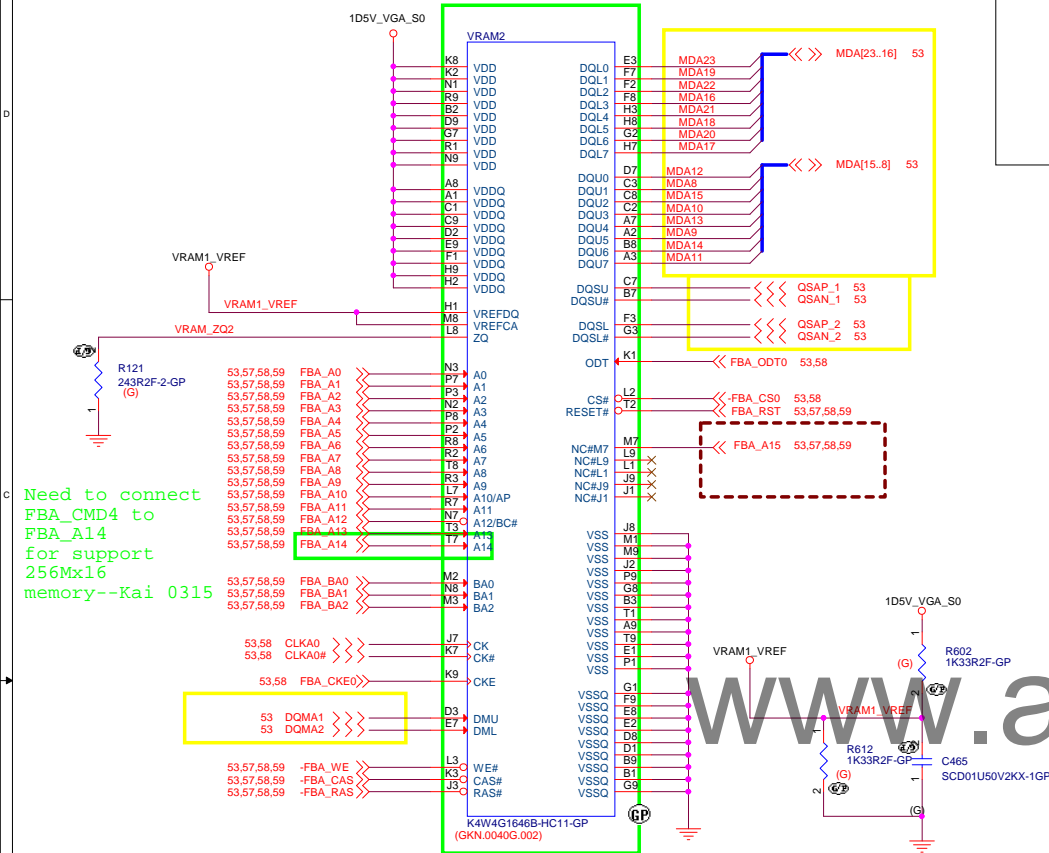
VDD_282

VDD_283

CHANNEL A:2GB DDR3

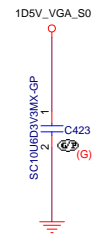
MICRON 256x16 900MHz 4Gb
MT41K256M16HA-107G:E LF+HF
KN.00404.001

Hynix 256x16 900MHz 4Gb
H5TQ4G63MFR-11C
KN.0040G.006



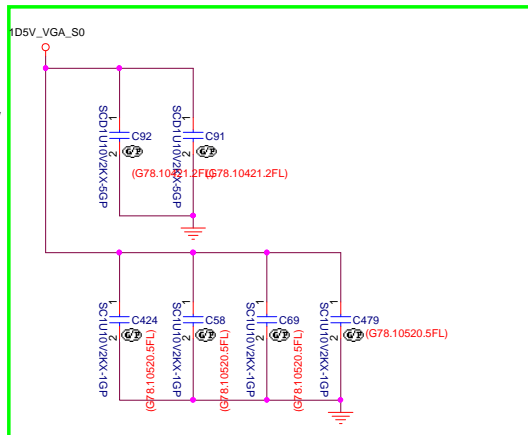
www.aitech1.ru

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

FOR VRAM1



Add VRAM decoupling cap--Kai 0315

<Core Design>

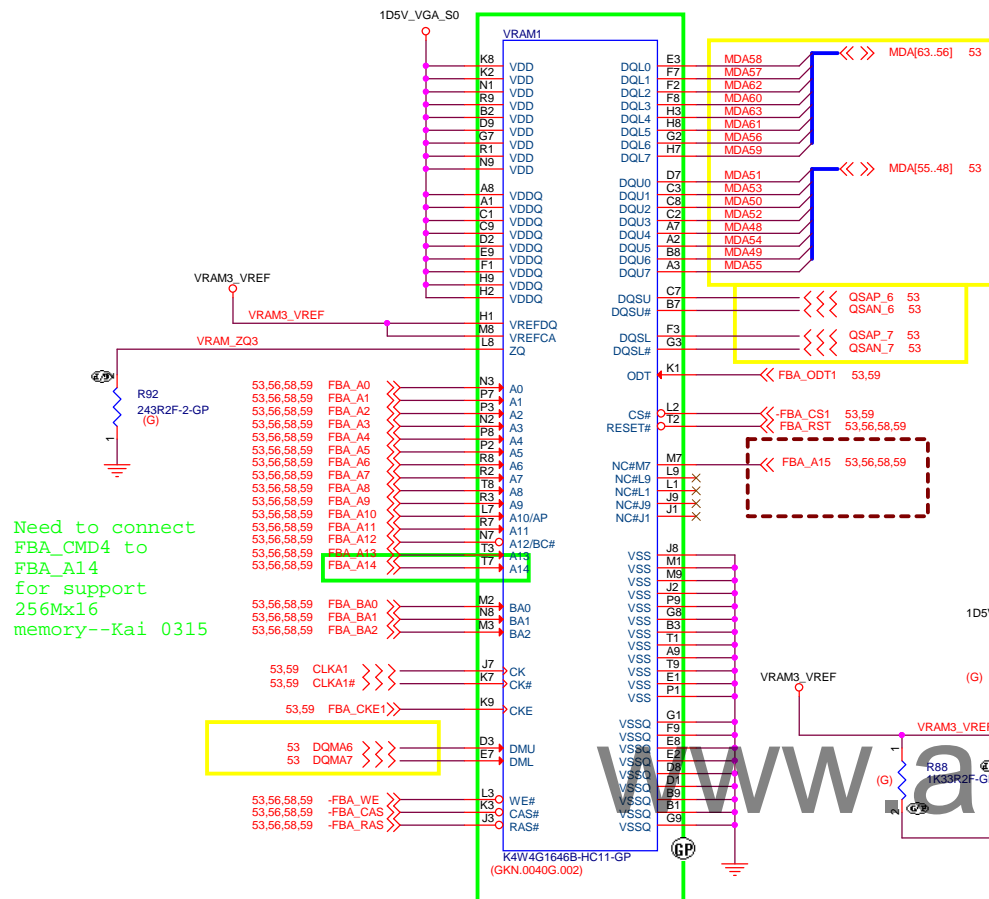
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

GPU-VRAM1 (1/4)			
Title	Document Number	Rev	SA
Size	Custom	Madrid	
Date:	Tuesday, January 21, 2014	Sheet	56 of 68

CHANNEL A:2GB DDR3

MICRON 256x16 900MHz 4Gb
MT41K256M16HA-107G:E LF+HF
KN.00404.001

Hynix 256x16 900MHz 4Gb
H5TQ4G63MFR-11C
KN.0040G.006



Need to connect
FBA_CMD4 to
FBA_A14
for support
256Mx16
memory--Kai 0315

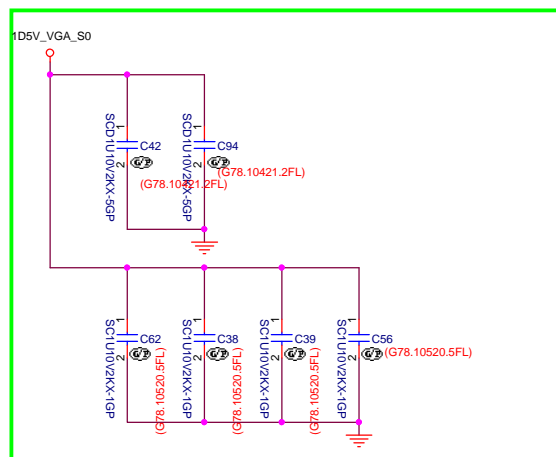
OBS,follow Lily_Tripoli--Kai 0311

FB CMD mapping Mode D-N12x

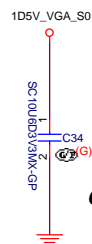
VRAM SAMSUNG 1Gb S72.41646.Q0U
VRAM HYNIX 1Gb H72.51G63.H0U

FOR VRAM3

CLOSE TO THE MEMORY



Add VRAM decoupling cap--Kai 0315

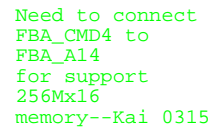


CLOSE TO THE MEMORY

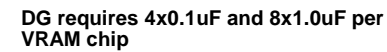
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM3 (2/4)			
Size Custom	Document Number		Rev SA
Madrid			
Date: Tuesday, January 21, 2014	Sheet 57	of 68	

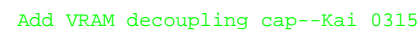

```
Hynix 256x16 900MHz 4Gb
H5TQ4G63MFR-11C
KN.0040G.006
```



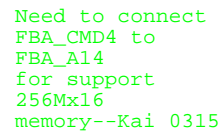
www.aitech1.ru



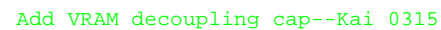
CLOSE TO THE MEMORY




```
Hynix 256x16 900MHz 4Gb
H5TQ4G63MFR-11C
KN.0040G.006
```

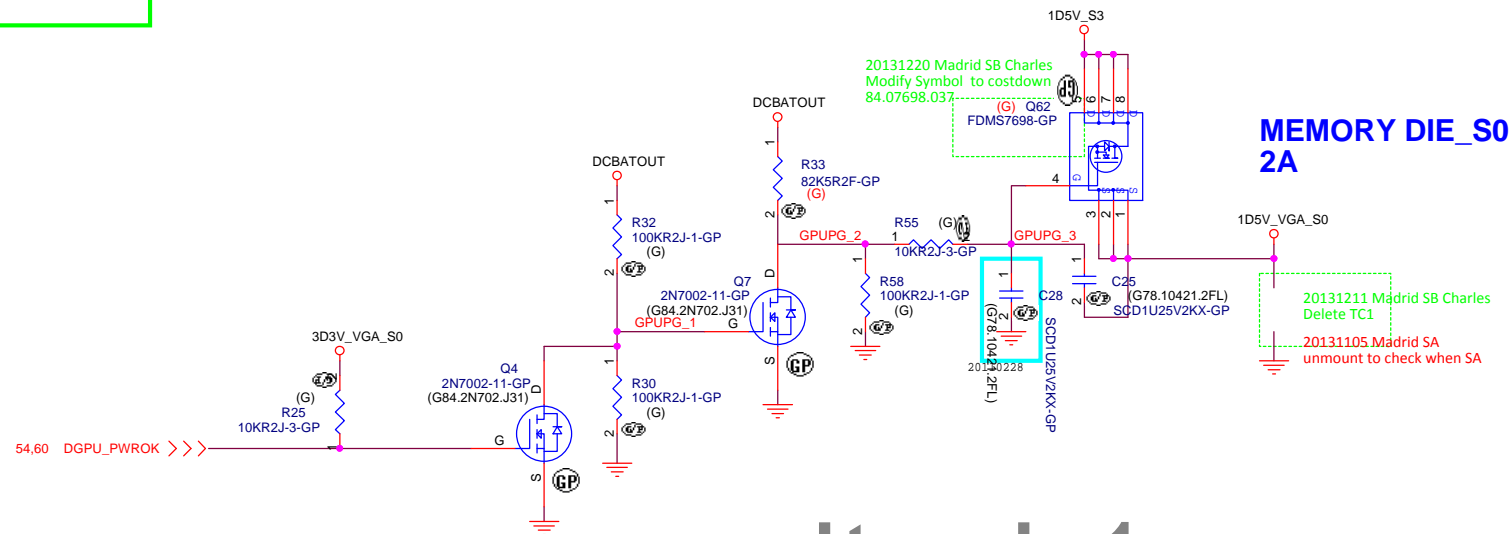


CLOSE TO THE MEMORY



1D5V_VGA_S0
MAX=6A

GPU VCORE -> MEMORY POWER



www.aitech1.ru

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU PWR 1D5V VGA(51363)

Size

Document Number

Custom

Madrid

Date:

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Rev

SA

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of

68

Power Sequencing Requirement N15S-GT-B-A2

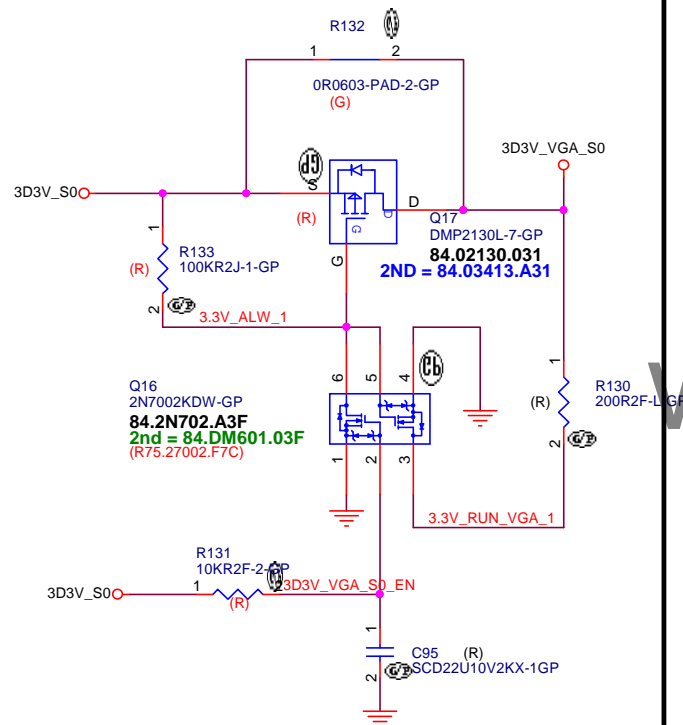
Power-on:

3D3V_VGA_S0-->NVVDD==1D05V_VGA_S0-->1D5V_VGA_S0

Power-off:

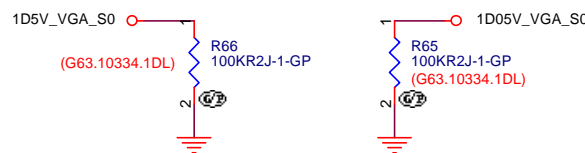
The timing of all power rail need power down to 0V under 10ms.

+3VS to 3.3V_DELAY Transfer



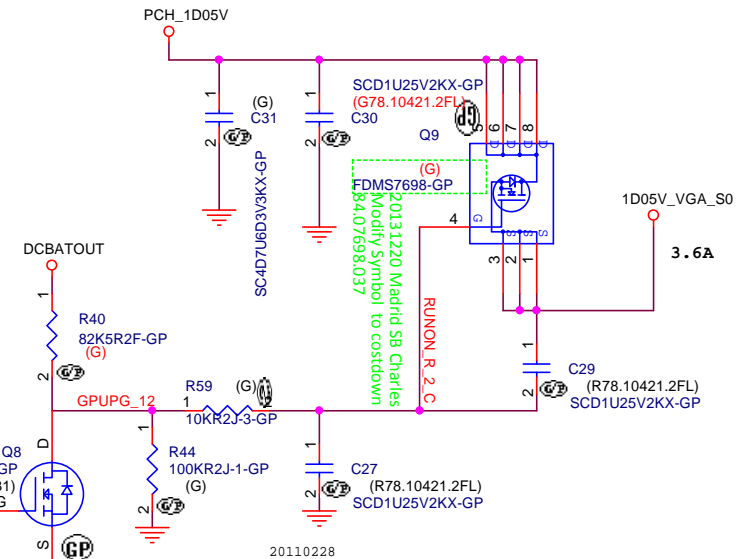
www.aitech1.ru

60 PWR_VGA_CORE_EN >>>



1.05V to 1.05V_VGA_S0 Transfer

FDMS0310, POWER PAK
Max Rdson=3.5m ohm at Vgs=10V,21A



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU PWR 1D05V/3D3V

Size

Document Number

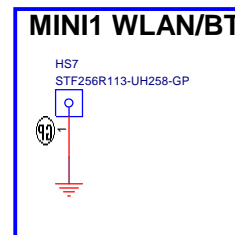
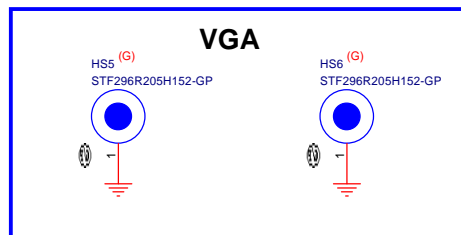
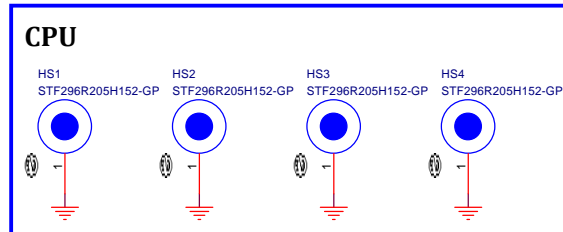
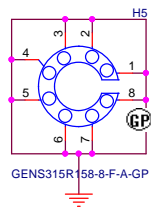
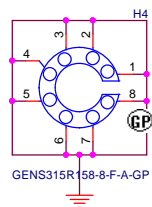
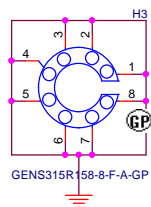
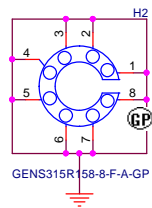
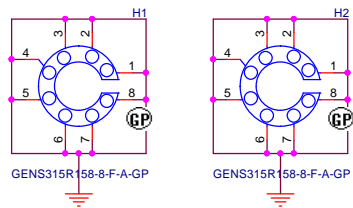
Madrid

Rev

SA

Date: Tuesday, January 21, 2014

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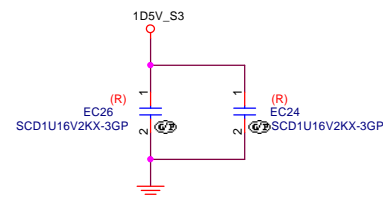
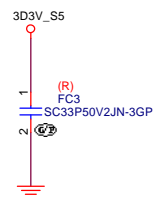
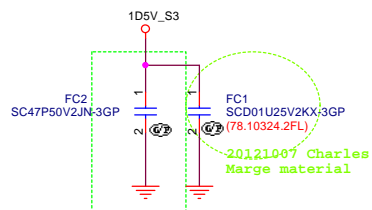
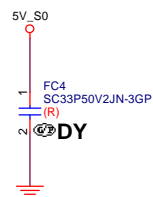
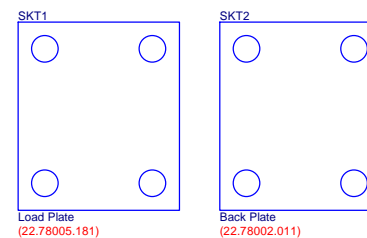


34.3HJ02.001 -> 1.5mm
34.3KF01.001 -> 3.3mm
34.3HJ03.001 -> 6.5mm
34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41

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2012/09/10_aPisa_SA
2012/09/30_aPisa_SB
Modify H4 symbol

CPU Plate



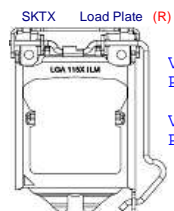
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	STAND OFF/HOLE/EMI CAP		
Size A3	Document Number	Rev SA	
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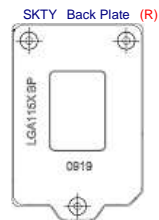
Material part

LGA115x CPU SOCKET Symbol



Vendor: LOTES
P/N: 22.78003.011

Vendor: FOXCONN
P/N: 22.78006.001



Vendor: LOTES
P/N: 22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)

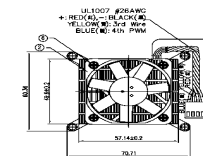
Vendor: FOXCONN
P/N: 22.78006.011
Thickness: 2.0mm (含mylar)



Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

HeatSink+FAN Symbol



Vendor
P/N:

HSFAN1
(R60.3KN01.001)

LABEL



LBL1
LABEL
(45.41107.011)

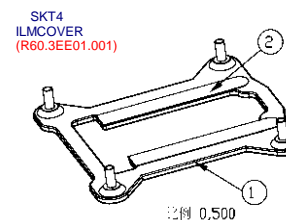
MB serial NO# and MAC address
45.41101.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm



LBL2
LABEL
(R)



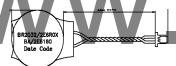
LBL3
LABEL
(R)



Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

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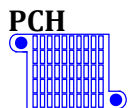


BAT1
BATTERY CR2032_30MM
(R23.21221.024)

Wire Length: 30mm

Vendor
P/N:
23.21221.024
23.21212.031

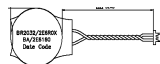
HeatSink Symbol



PCHHS1
HEATSINK
(60.3MN01.001)

Vendor
P/N: Pisa2
60.3ET05.001
60.3ET05.011
60.3ET05.021

Vendor
P/N: Madrid
60.3MN01.011 (second source)
60.3MN01.001



BAT2
BATTERY BR2032_60MM
(R23.24220.612)

Wire Length: 60mm
耐高温>85C

Vendor
P/N:
23.21208.061
23.24220.612

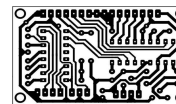
Battery Symbol



BAT3
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

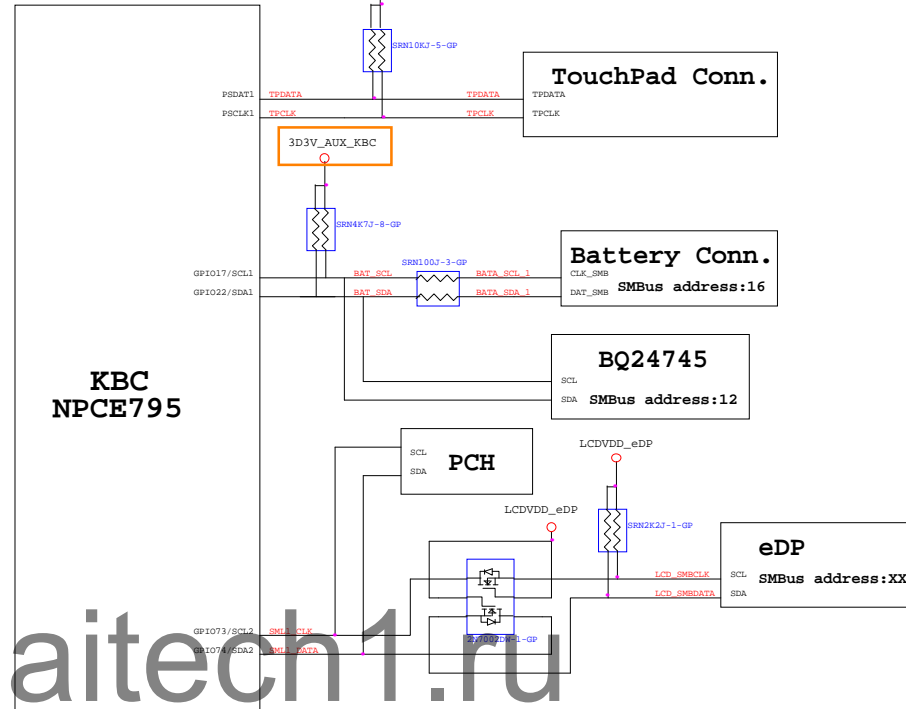
PCB Symbol



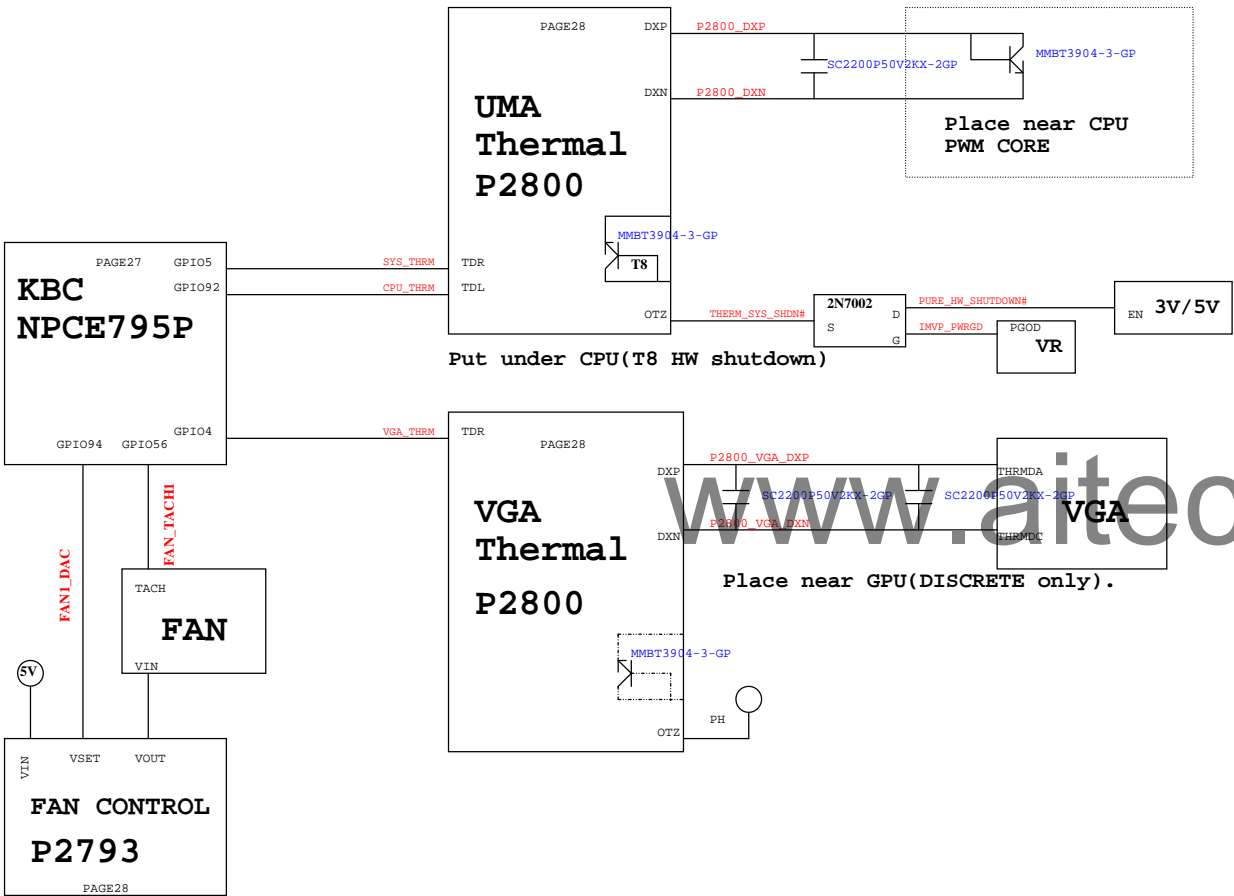
PCB1
PCB
(R)

wistron [®]		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title HeatSink / Battery cell /etc			
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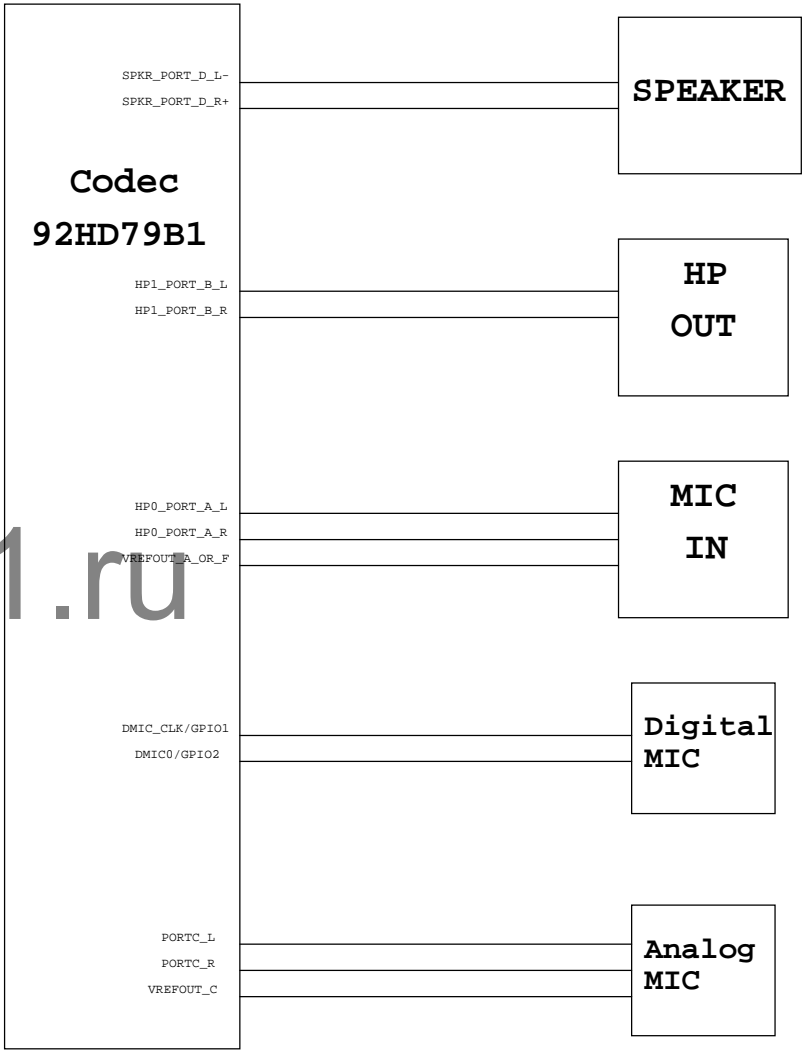
KBC SMBus Block Diagram

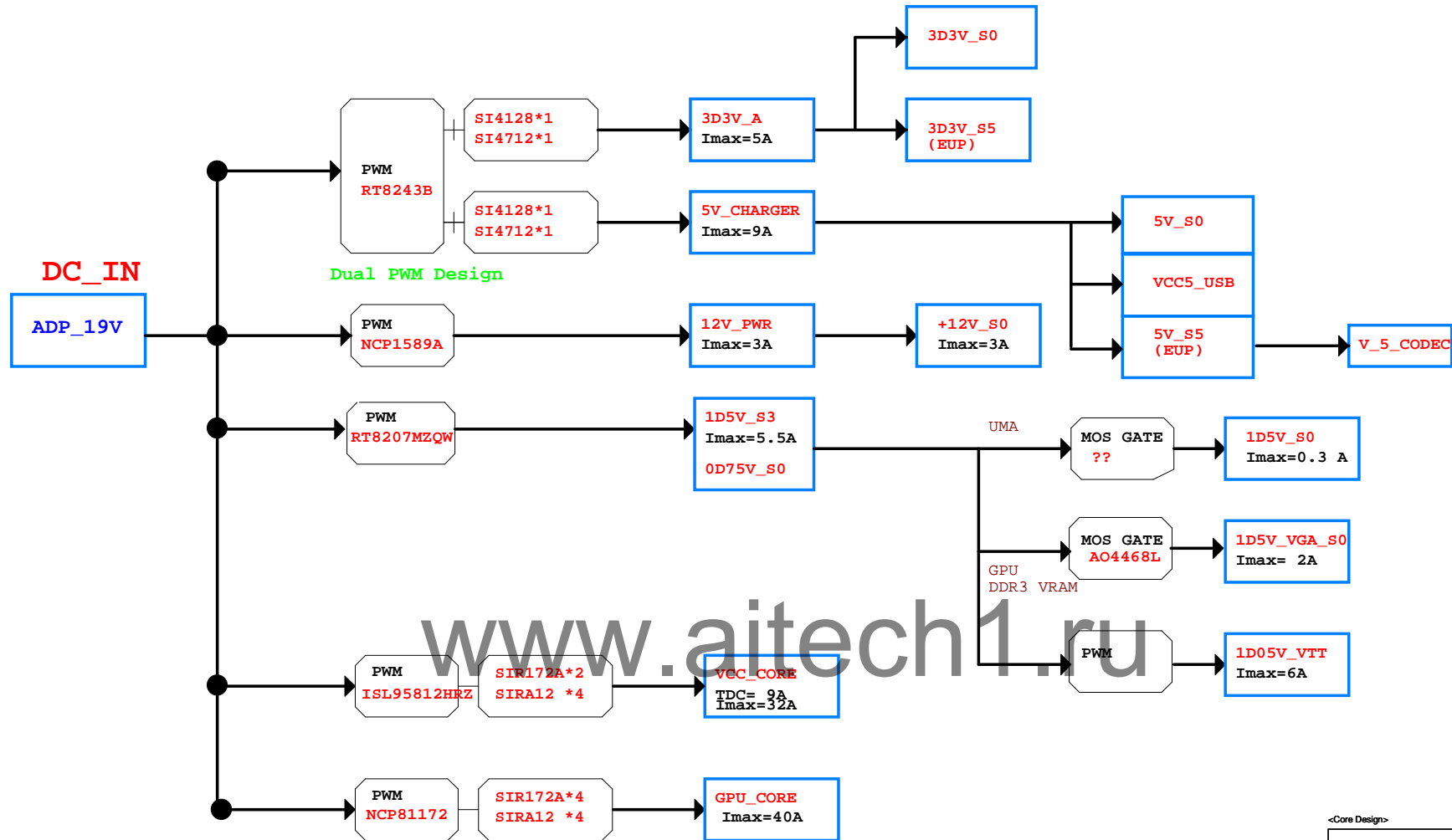


Thermal Block Diagram



Audio Block Diagram





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size	
Custom	
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